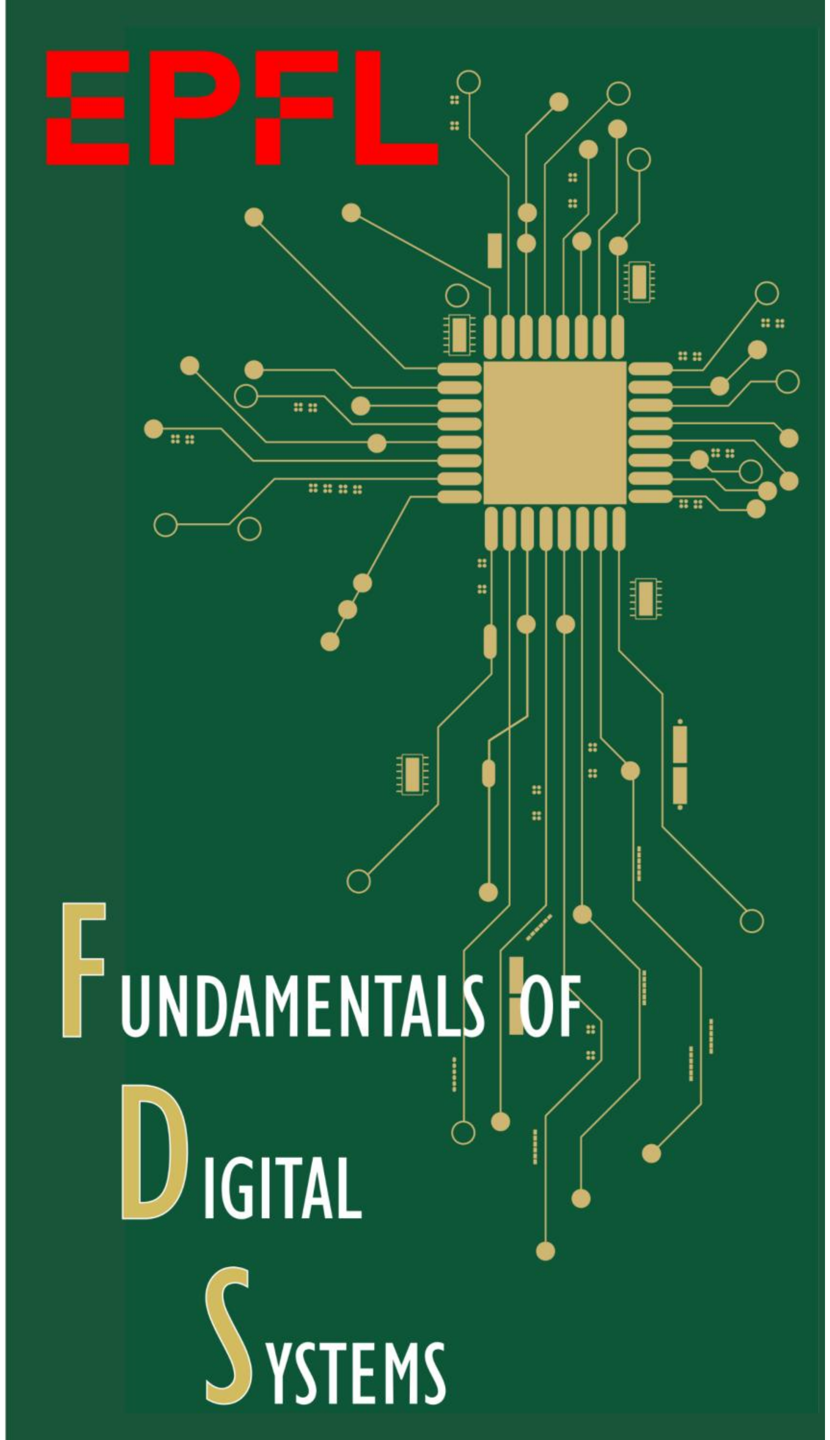


Digital Logic Circuits

Timing Analysis of Synchronous Circuits

CS-173 Fundamentals of Digital Systems

Mirjana Stojilović

Spring 2025

Previously on FDS

Registers and Counters

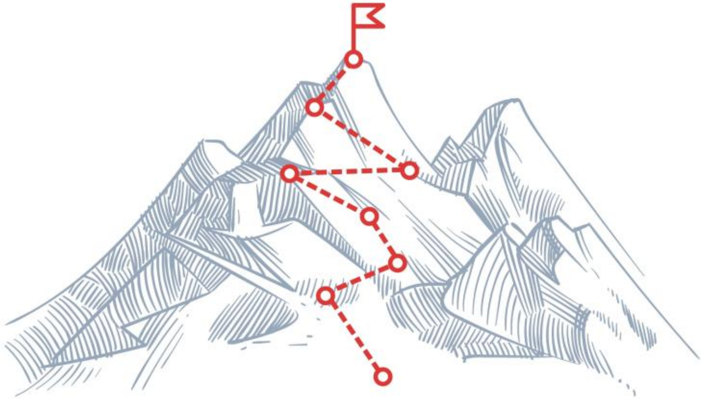
Previously

- Grouping FFs in a register
  - Composing shift registers
    - Serial-in, serial-out
    - Parallel-in, parallel-out
  - Creating counters
- Verilog, contd.
  - For loops
  - Operators
    - Logical
    - Relational
    - Equality

Let's Talk About…

Timing Analysis of Synchronous Circuits

Learning Outcomes



- Discover flip-flop timing constraints and parameters
  - Setup and hold
  - Clock-to-Q
- Be aware of timing issues related to the clock—the skew
- Perform timing analysis, taking into account the timing constraints
- Understand metastability and how to handle it

Quick Outline

- FF Timing Contraints and Parameters
- Life of D
- Meeting setup time
  - Algorithm
- Meeting hold time
  - Algorithm
- Example: Timing analysis
- Clock Skew
- Life of D, revisited
- Meeting setup time
- Meeting hold time
- Implications of clock skew
- Example: With clock skew
- Metastability

Flip-flop Timing Constraints and Parameters

Synchronous System Design

- In practical circuits, the outputs of sequential logic elements (registers) connect to the inputs of other sequential logic elements
- Typically, there is some combinational logic between FFs, which implements the circuit functionality and, inevitably, introduces delays
- For correct circuit operation, **timing constraints must be met**

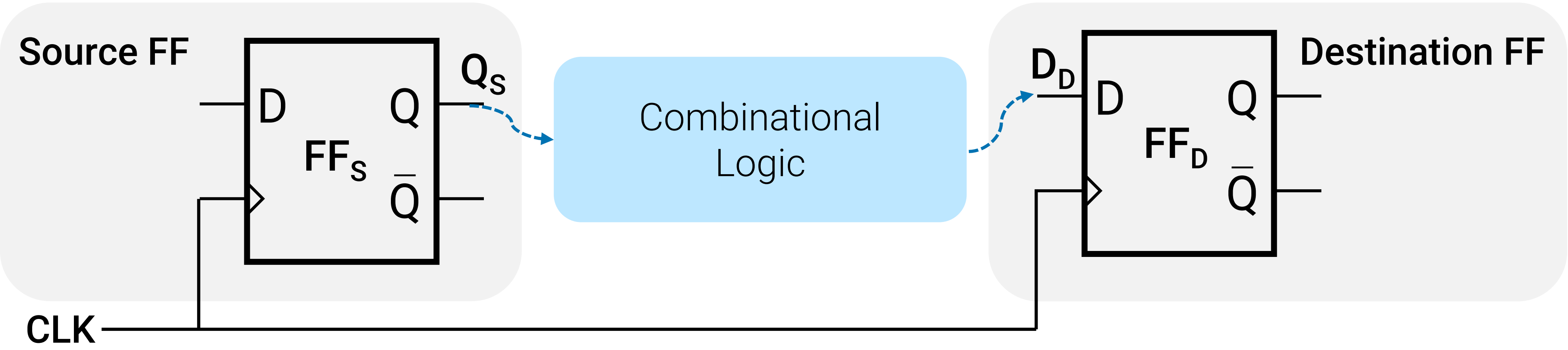


Fig. Generic structure of a synchronous system

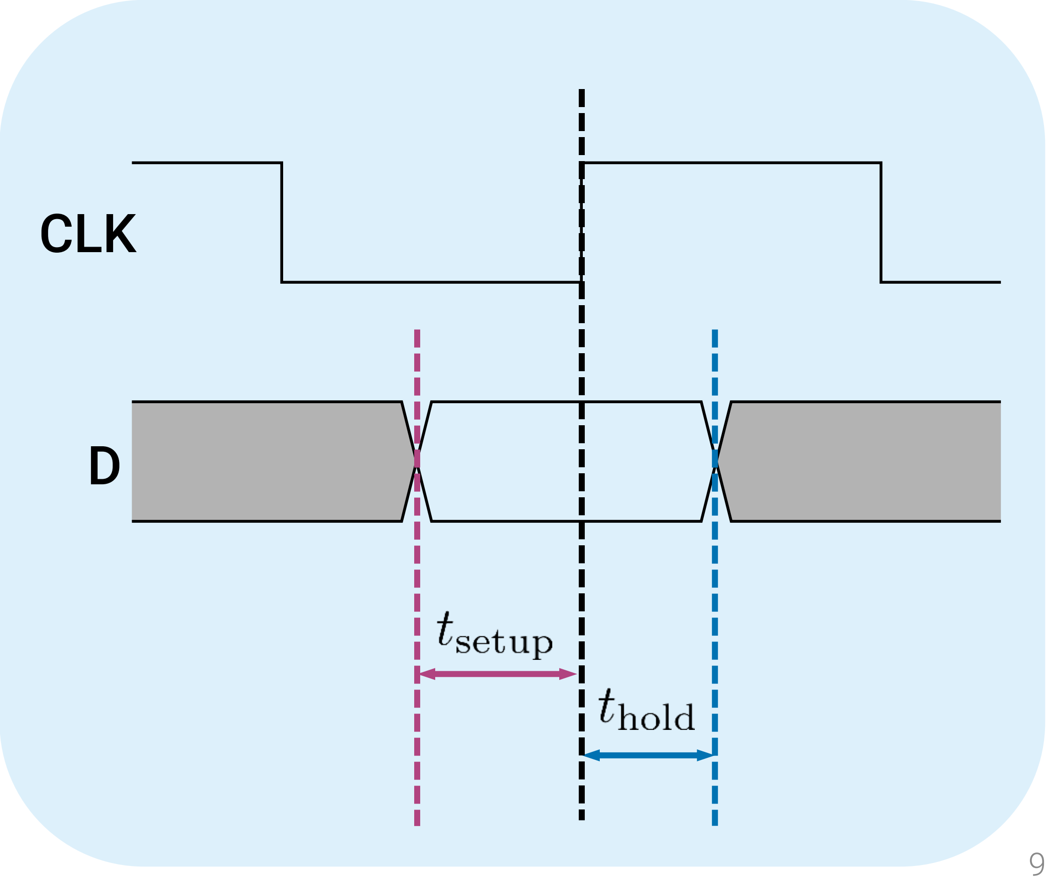
D Flip-Flop Input Timing Constraints

- Signal on input D of a DFF must be stable around the **active** clock edge

- D must be stable during
  - **Setup** time: time **before** the active clock edge
  - **Hold** time: time **after** the active clock edge

- Otherwise, the input timing constraints are not satisfied

- Violating the input timing constraints leads to **metastability**



Metastability

- If the signal on the data input D of a FF is not stable around the active clock edge (during the setup time or hold time), metastability can occur

- Metastability behavior:
    - First, the output of the FF gets stuck at a voltage level between 0 and 1
    - Later, the output settles to logic 0 or 1, in a nondeterministic (random) manner

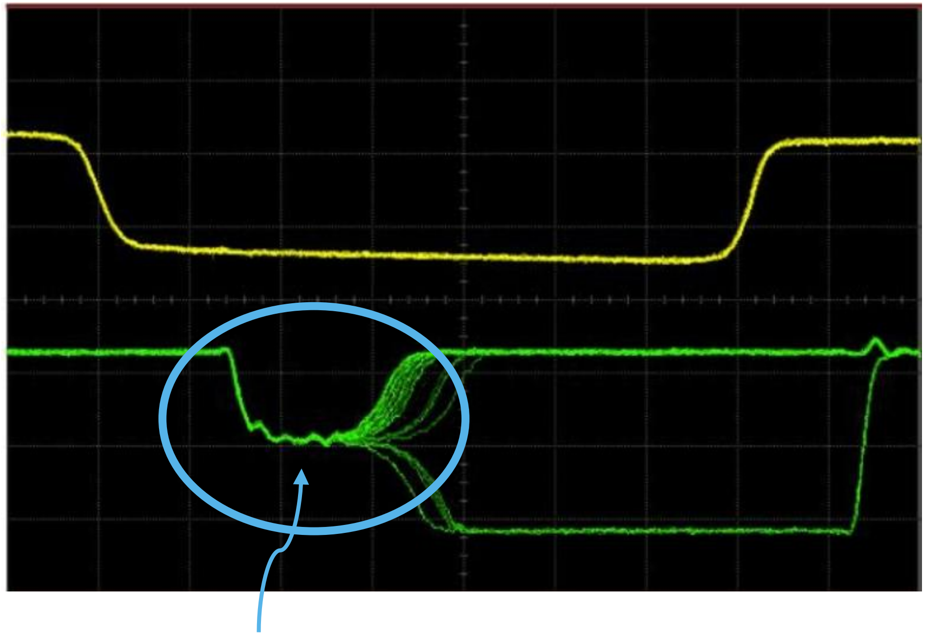
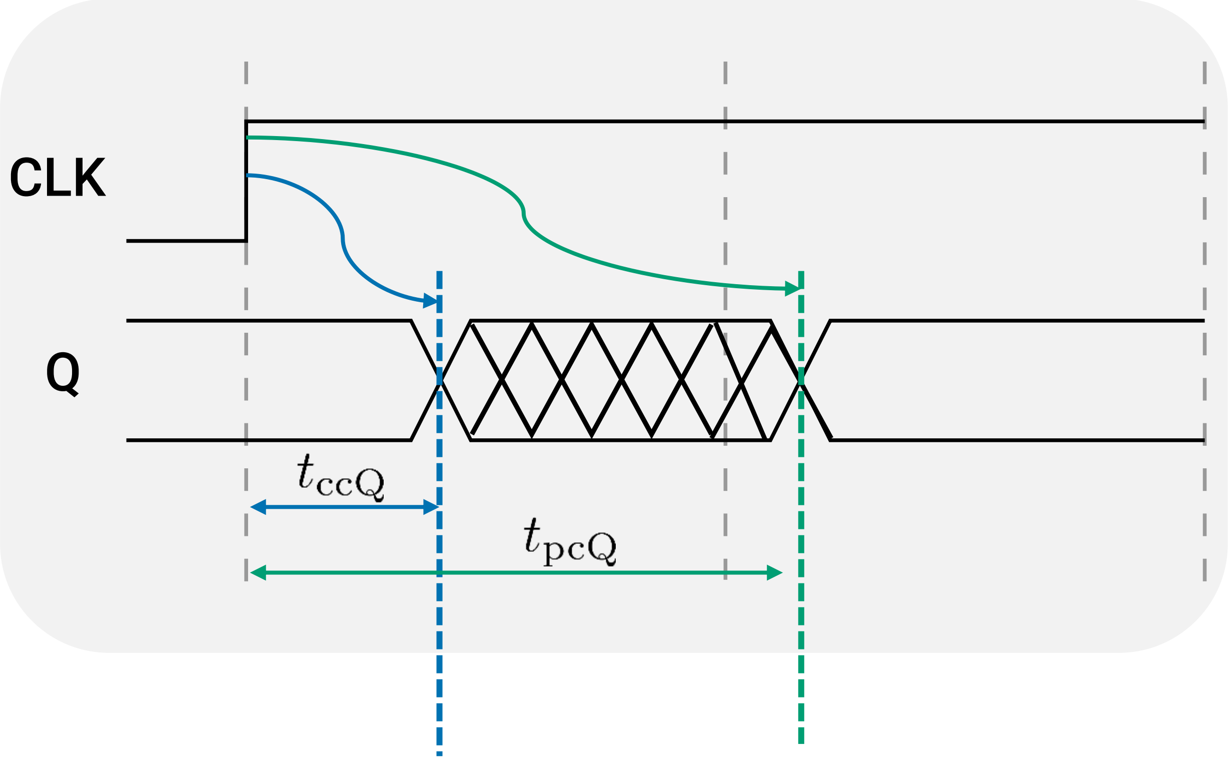


Image source: W. J. Dally, Lecture notes
Metastability and Synchronization Failure, 2005

D Flip-Flop Output Timing Parameters

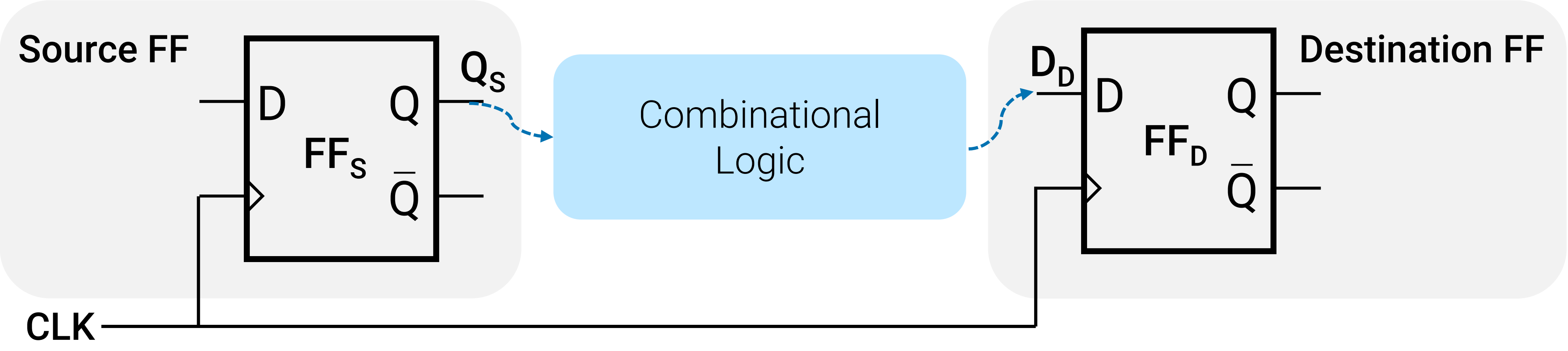
- FF timing properties (not constraints)
- Contamination delay **clock-to-q** is the earliest after the clock edge that the output Q starts changing
- Propagation delay **clock-to-q** is the latest after the clock edge that the output Q stops changing
- We can combine the above two timing parameters under one name
  - t_{cQ}, clock-to-Q delay



$t_{cQ,\min} = t_{\text{ccQ}}$ $\quad t_{cQ,\max} = t_{\text{pcQ}}$

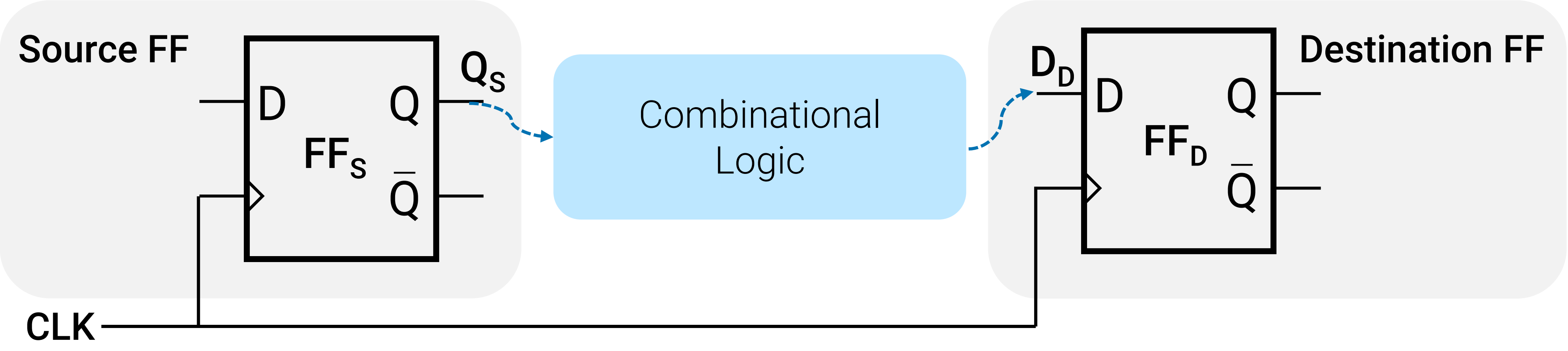
Meeting FF Timing Constraints

- The outputs of sequential logic elements connect to the inputs of other sequential logic elements
- For correct operation, all **"FF output" to "FF input"** paths in the circuit must meet timing constraints



Meeting FF Timing Constraints

- We must ensure the correct timing of all D inputs in our circuit
- The value at the input of the FF must be stable for
  - At least t_{setup} **before** the active clock edge
  - At least t_{hold} **after** the active clock edge



Life of D

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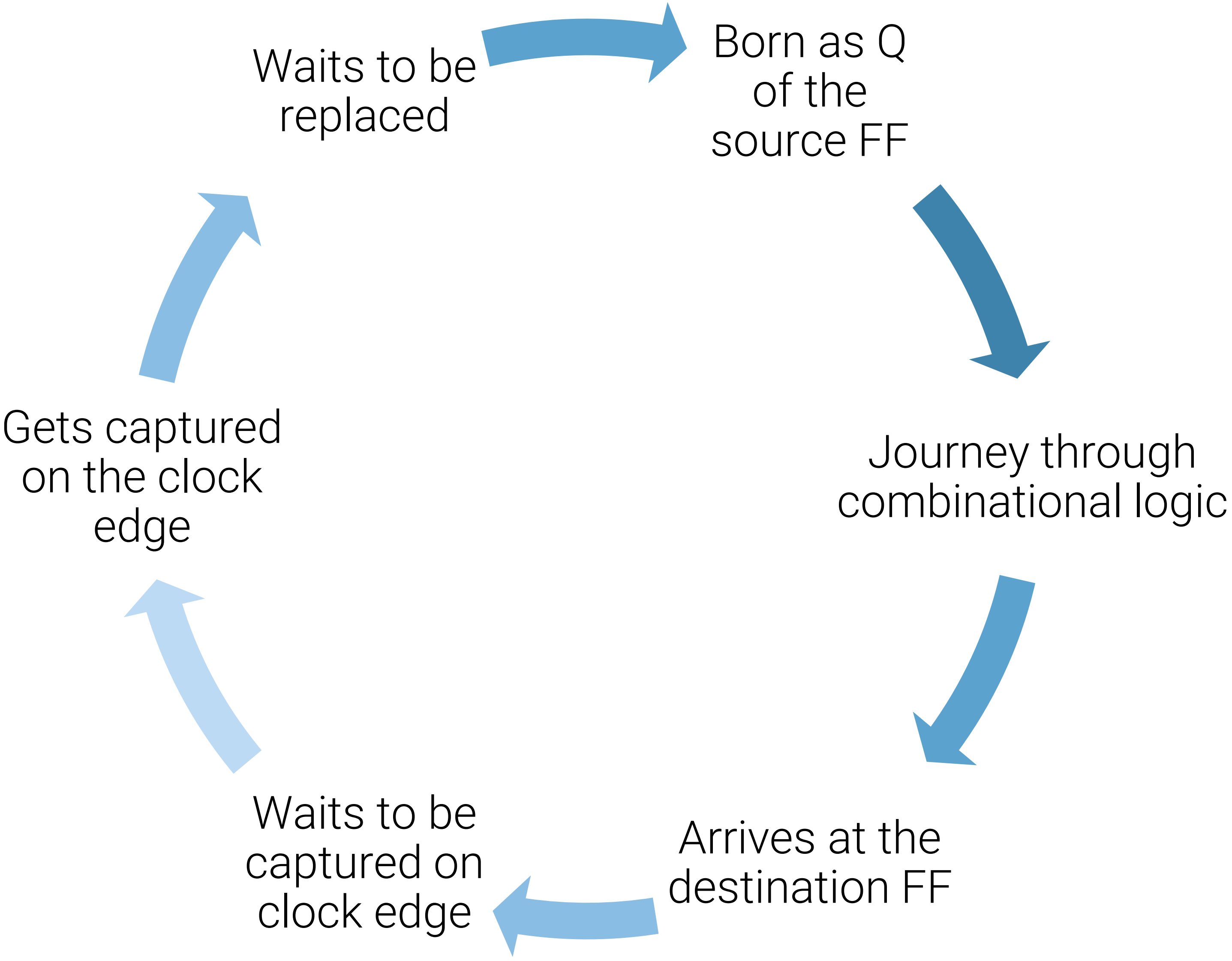
Life of D

Lasting One Clock Cycle



Born as Q of the source FF

Journey through combinational logic

Arrives at the destination FF

Waits to be captured on clock edge

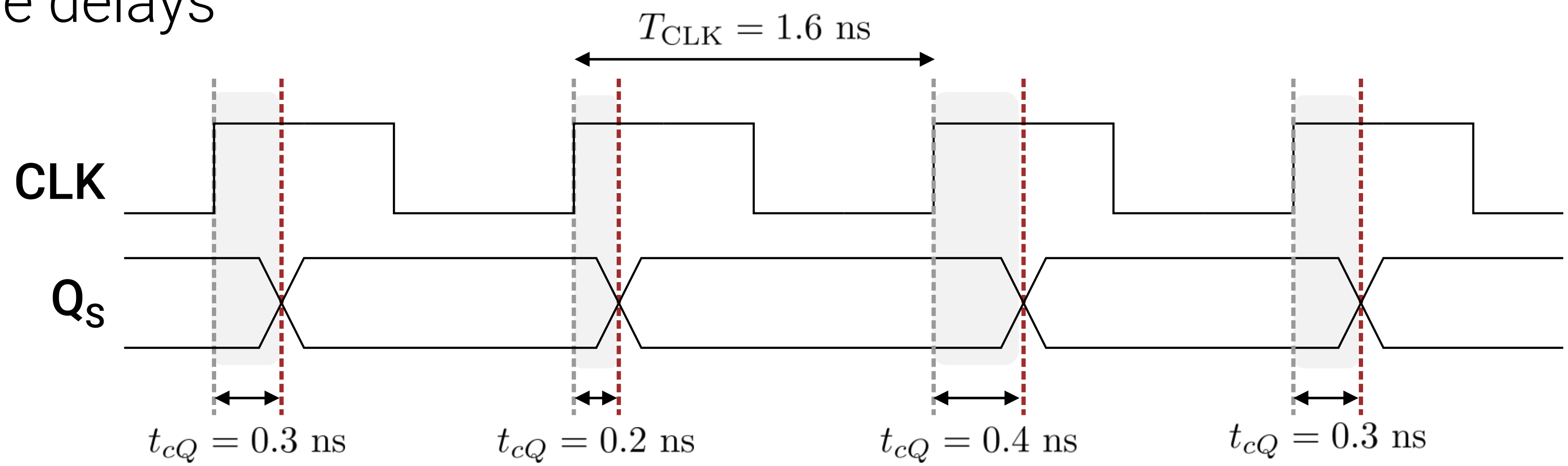
Gets captured on the clock edge

Waits to be replaced

Born as Q of a Source DFF

And to get born took some time…clock-to-Q

- For an arbitrary sequence of values on the input D of the FF, the output Q changes after the clock-to-Q delay; clock-to-Q delay can be any value in the range between $t_{cQ,\min}$ and $t_{cQ,\max}$
- Example delays

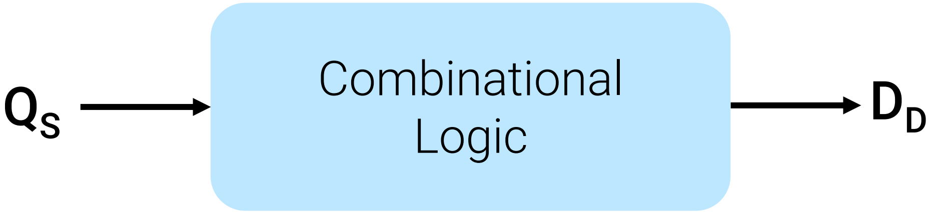


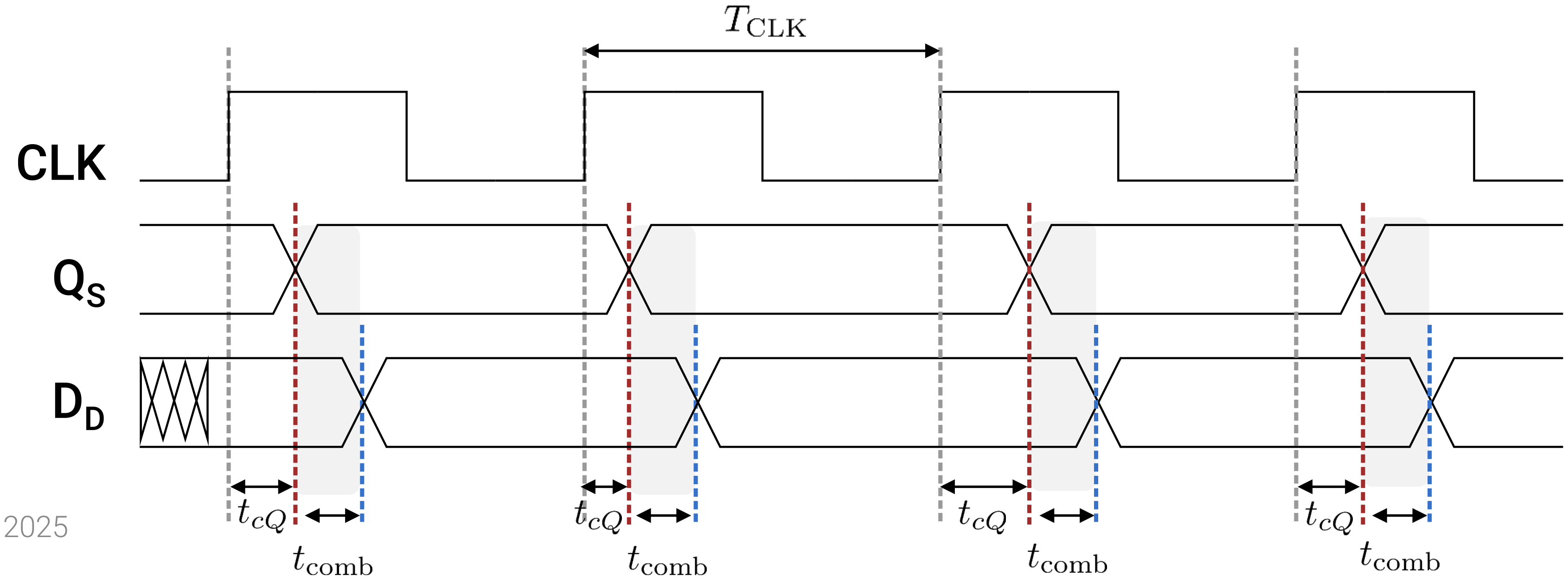
Updating the output of the source FF (Q_S) takes some (variable) clock-to-Q delay

Journey Through Combinational Logic

Wild ride…

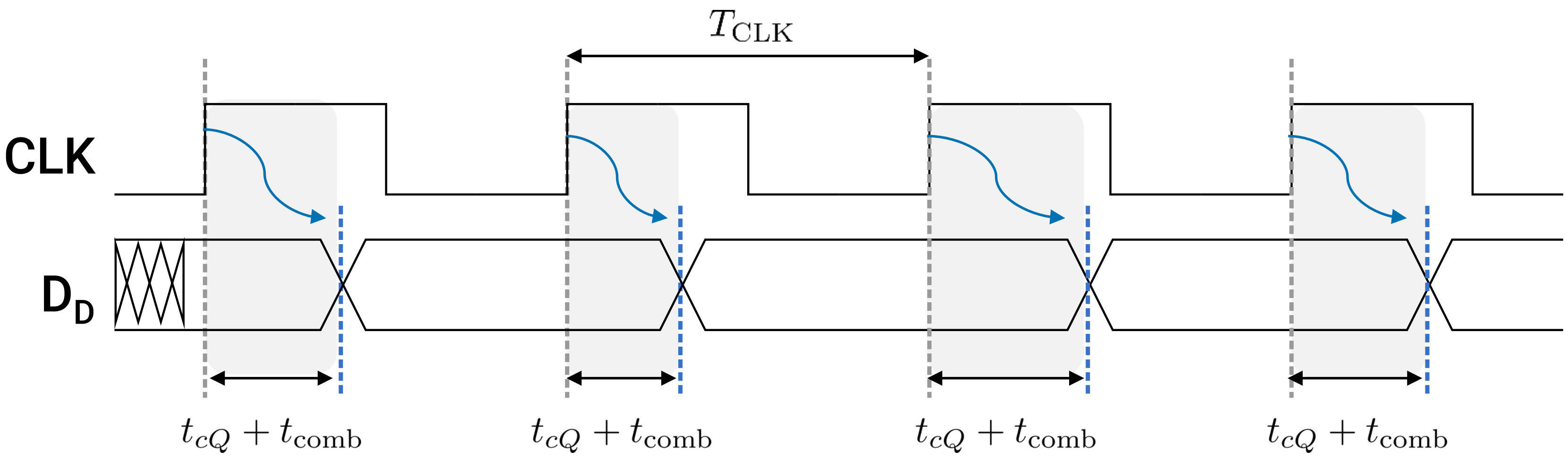
- D starts the journey as Q_S
- Ends the journey as D_D
  - Input of the destination FF
- Duration of the journey: t_{comb}





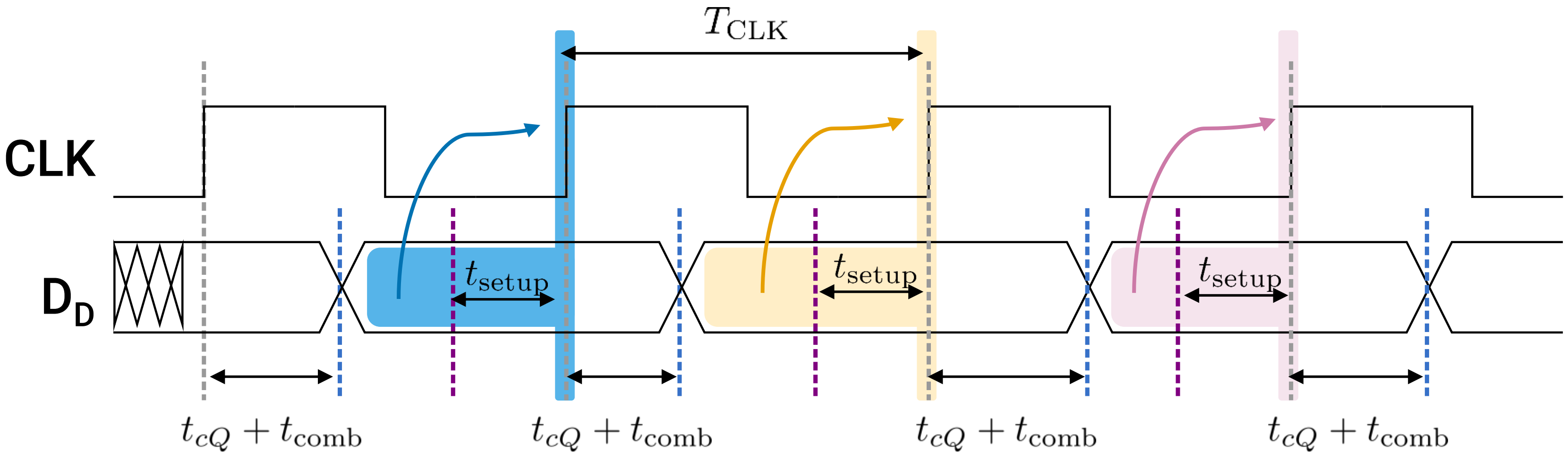
Arrives at the Destination FF

- After, in total, $t_{cQ} + t_{\mathrm{comb}}$


T_{CLK}
CLK
$\mathrm{D_D}$
$t_{cQ} + t_{\mathrm{comb}}$
$t_{cQ} + t_{\mathrm{comb}}$
$t_{cQ} + t_{\mathrm{comb}}$
$t_{cQ} + t_{\mathrm{comb}}$

Waits…

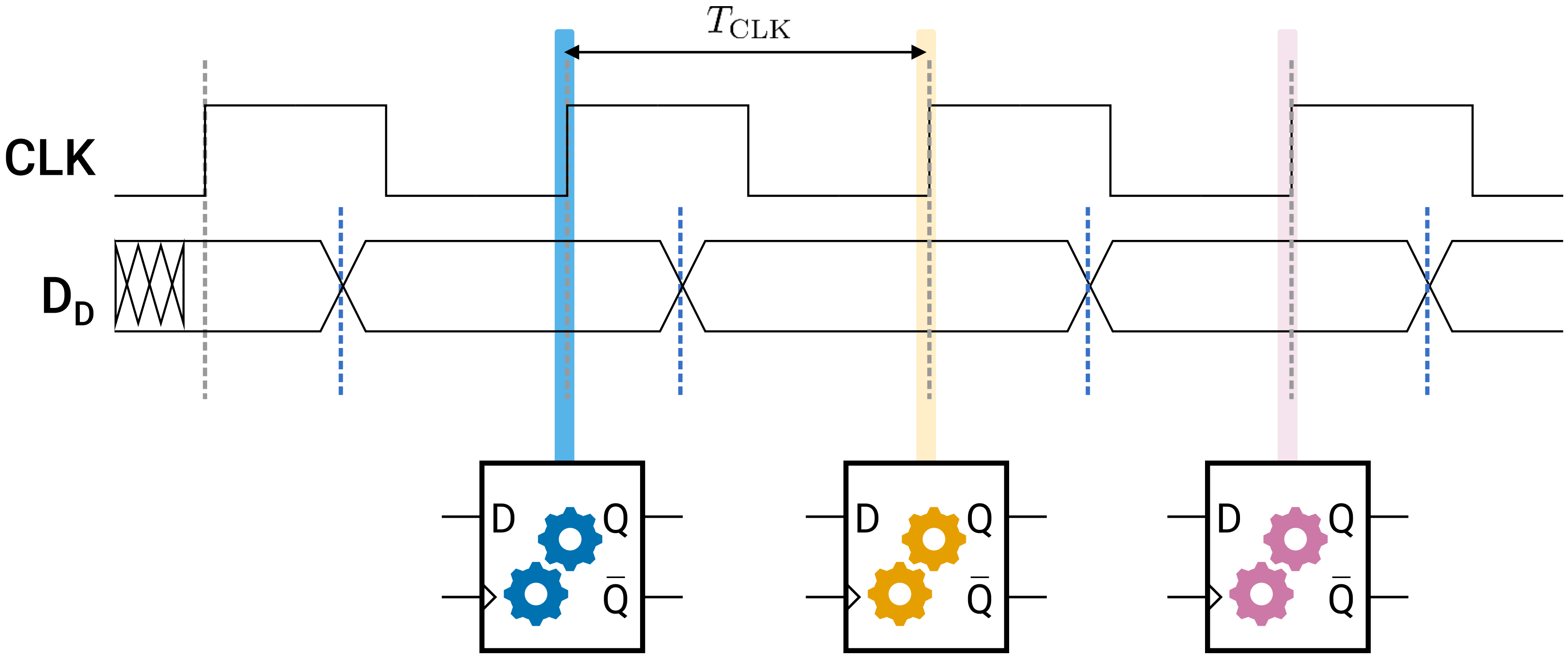
- …to be captured by the **next** clock edge


T_{CLK}
CLK
D_D
t_{setup}
t_{setup}
t_{setup}
$t_{cQ} + t_{\mathrm{comb}}$
$t_{cQ} + t_{\mathrm{comb}}$
$t_{cQ} + t_{\mathrm{comb}}$
$t_{cQ} + t_{\mathrm{comb}}$

- During the “wait”, D_D should be stable
- The wait must be at least as long as the setup time t_{setup} for the destination FF to capture D correctly

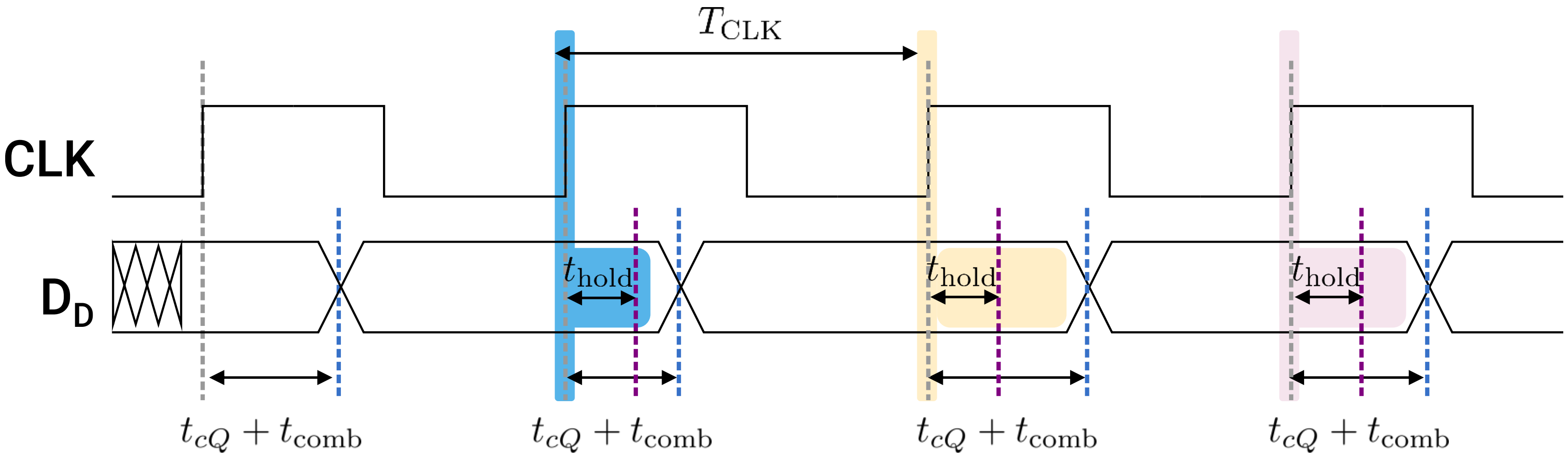
Gets Captured on the Clock Edge

- The destination FF takes the value on D_D and “works” on memorizing it and passing it to the output Q_D



D Waits…

- …to be replaced. The clock edge that captured is passed…

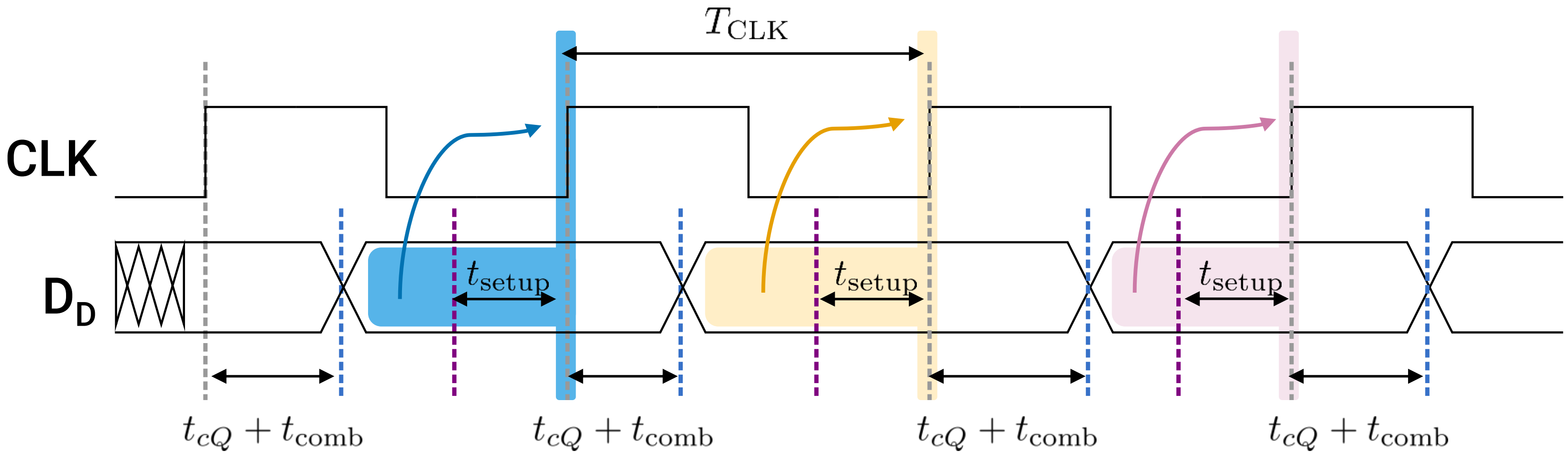

T_{CLK}
CLK
$\mathrm{D_D}$
t_{hold}
t_{hold}
t_{hold}
$t_{cQ} + t_{\mathrm{comb}}$
$t_{cQ} + t_{\mathrm{comb}}$
$t_{cQ} + t_{\mathrm{comb}}$
$t_{cQ} + t_{\mathrm{comb}}$

- The "wait" must be at least as long as the hold time t_{hold} for the destination FF to capture $\mathrm{D_D}$ correctly

Meeting Timing Constraints

Checking for Setup and Hold Time Violations

Meeting Setup-Time Constraints


T_{CLK}
CLK
D_D
t_{setup}
t_{setup}
t_{setup}
$t_{cQ} + t_{\text{comb}}$
$t_{cQ} + t_{\text{comb}}$
$t_{cQ} + t_{\text{comb}}$
$t_{cQ} + t_{\text{comb}}$

- The following expression must hold for all possible values of t_{cQ} and t_{comb}:

$$T_{\text{CLK}} - (t_{cQ} + t_{\text{comb}}) \geq t_{\text{setup}}$$

- The worst-case constraint can be rewritten as

$$t_{cQ,\text{max}} + t_{\text{comb, max}} + t_{\text{setup}} \leq T_{\text{CLK}} = 1/f_{\text{CLK}}$$

Algorithm for Finding f_{max}

- Algorithm for finding f_{max}
  1. Identify all Q-to-D paths
  2. For every such path
     a. Compute its longest combinational delay
     b. Find the shortest clock period that satisfies the path's setup-time constraint
  3. Find the shortest clock period T_{CLK} that satisfies the setup-time constraints of **all** those paths
  4. Compute $f_{max} = 1/T_{CLK}$

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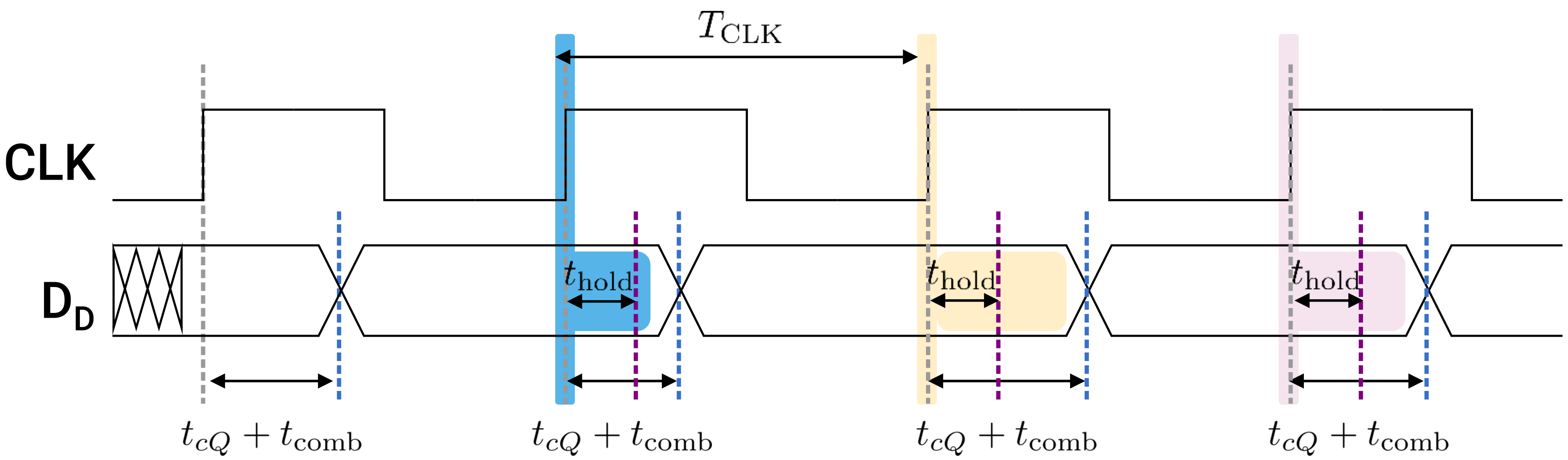
Meeting Hold-Time Constraints


T_{CLK}
CLK
D_D
t_{hold}
t_{hold}
t_{hold}
$t_{cQ} + t_{\text{comb}}$
$t_{cQ} + t_{\text{comb}}$
$t_{cQ} + t_{\text{comb}}$
$t_{cQ} + t_{\text{comb}}$

- The following expression must hold for all possible values of t_{cQ} and t_{comb}:

$$t_{cQ} + t_{\text{comb}} \geq t_{\text{hold}}$$

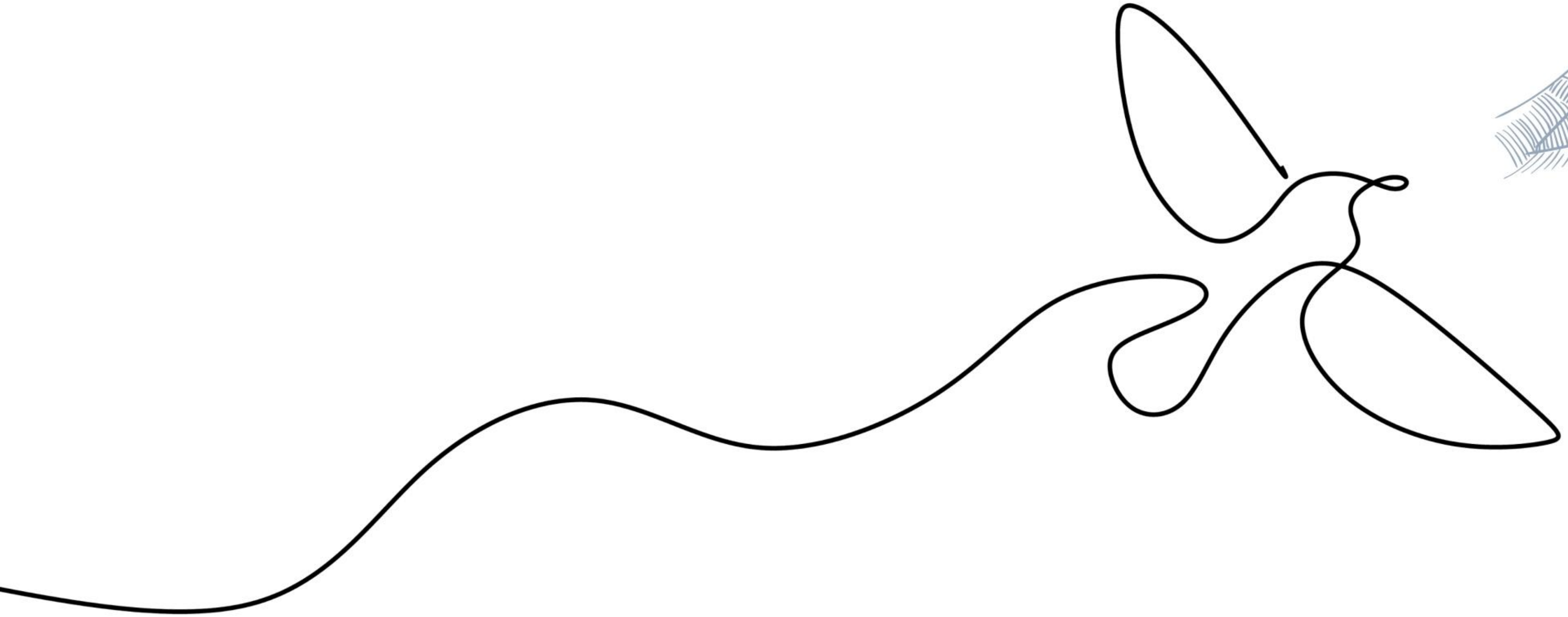
- The worst-case constraint can be rewritten as

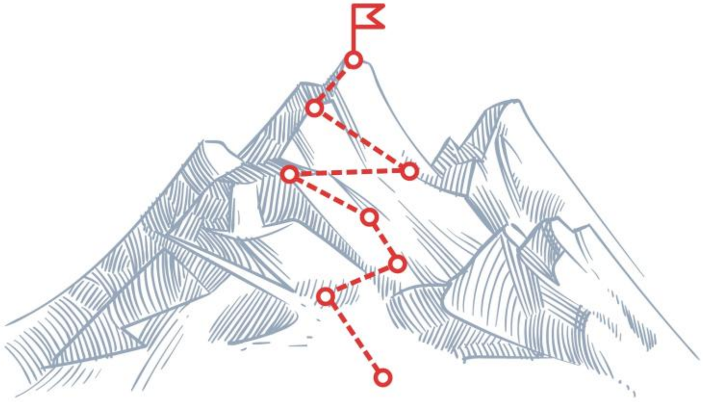
$$t_{cQ,\text{min}} + t_{\text{comb, min}} \geq t_{\text{hold}}$$

Algorithm for Checking Hold-Time Violations

- Algorithm for checking if hold-time constraints are satisfied
  1. Identify all Q-to-D paths
  2. For every such path
     a. Compute its shortest combinational delay
     b. Verify if hold-time constraint is satisfied

  Hold-time constraints must be satisfied for all Q-to-D paths





Example: Timing Analysis

Counter

EXAMPLES

Timing Analysis of a Counter

f_{max}, Hold-time violations

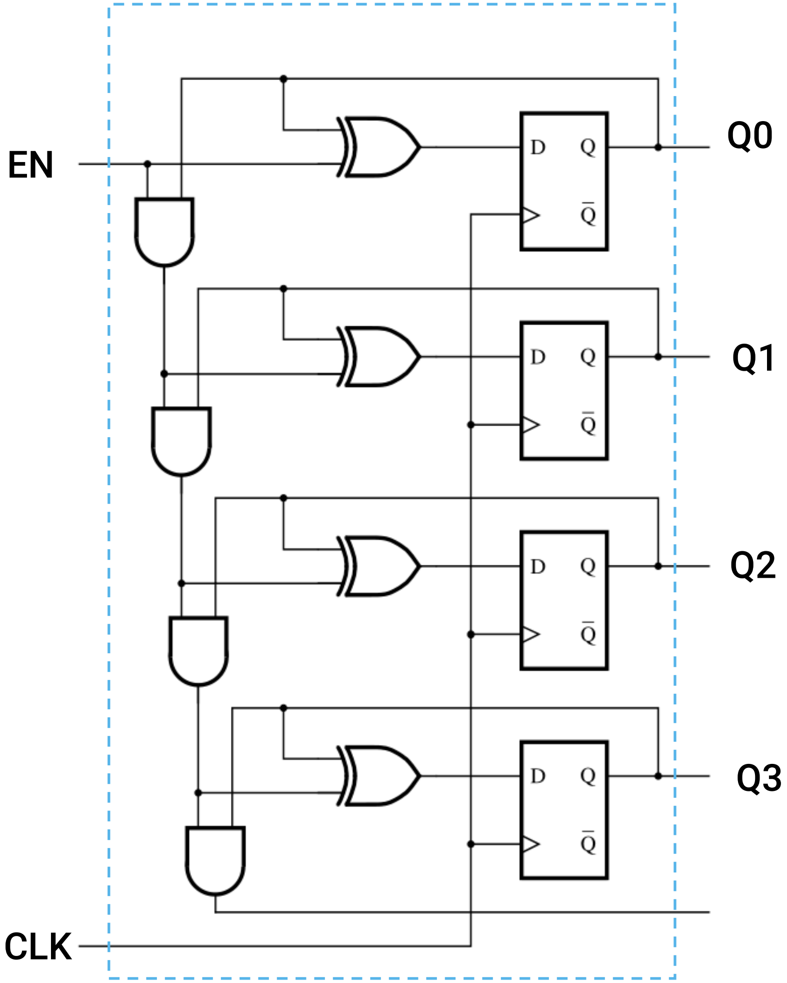
- Given the following FF timing constraints and parameters
  - $t_{\text{setup}} = 0.6 \text{ ns}$; $t_{\text{hold}} = 0.4 \text{ ns}$
  - $0.8 \text{ ns} \leq t_{\text{cQ}} \leq 1 \text{ ns}$

  and gate delays $t_{\text{AND}} = 1.2 \text{ ns}$ and $t_{\text{XOR}} = 1.3 \text{ ns}$

(a) Find the max operating frequency f_{max}

(b) Are there hold-time violations in this circuit?

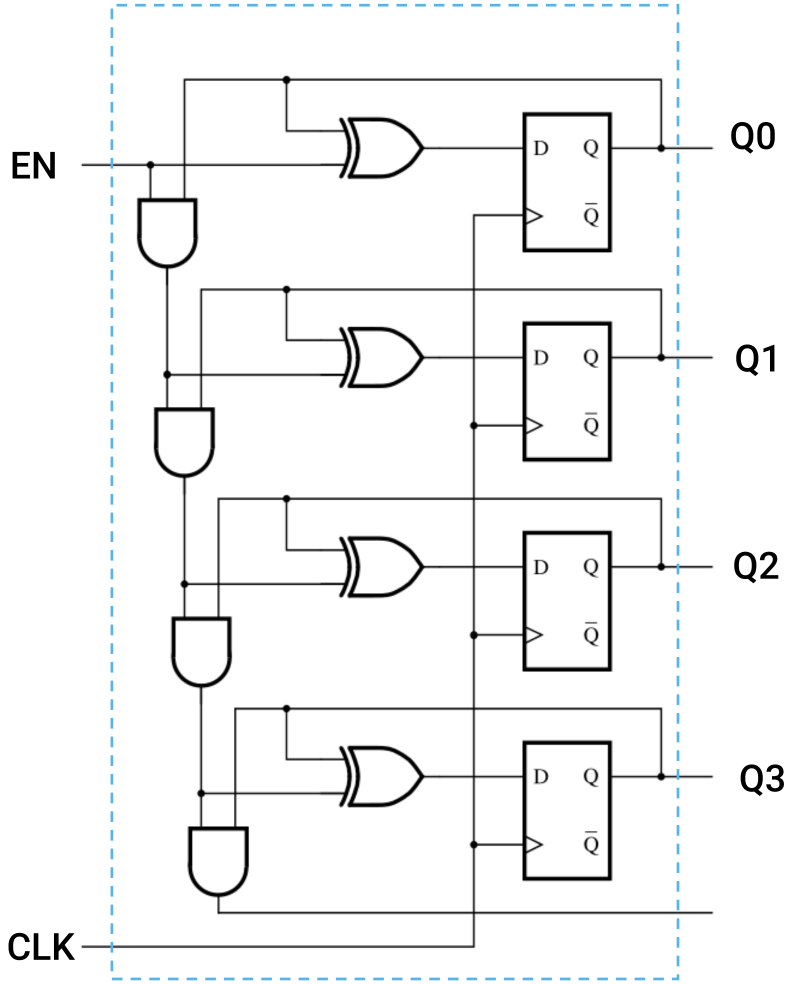
Note: For simplicity, we will assume that EN is available without delay



Timing Analysis of a Counter

f_{max}

- Step 1: Identify all Q-to-D paths
  - Q0 to D0
  - Q0 to D1
  - Q0 to D2
  - Q0 to D3
  - Q1 to D1
  - Q1 to D2
  - Q1 to D3
  - Q2 to D2
  - Q2 to D3
  - Q3 to D3

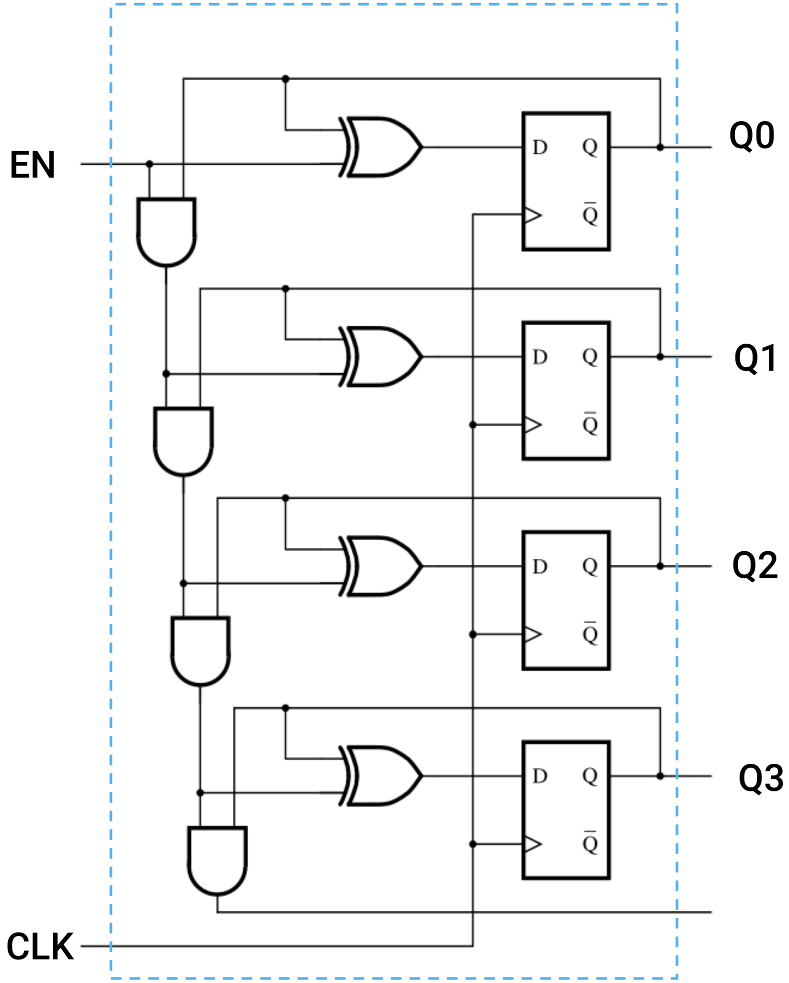


Timing Analysis of a Counter

f_{max}

- Step 2a: For each path, find longest comb. delay
  - Q0 to D0: $t_{\text{comb}} = t_{\text{XOR}} = 1.3\text{ ns}$
  - Q0 to D1: $t_{\text{comb}} = t_{\text{AND}} + t_{\text{XOR}} = 2.5\text{ ns}$
  - Q0 to D2: $t_{\text{comb}} = 2t_{\text{AND}} + t_{\text{XOR}} = 3.7\text{ ns}$
  - Q0 to D3: $t_{\text{comb}} = 3t_{\text{AND}} + t_{\text{XOR}} = 4.9\text{ ns}$
  - Q1 to D1: $t_{\text{comb}} = t_{\text{XOR}}$
  - Q1 to D2: $t_{\text{comb}} = t_{\text{AND}} + t_{\text{XOR}}$
  - Q1 to D3: $t_{\text{comb}} = 2t_{\text{AND}} + t_{\text{XOR}}$
  - Q2 to D2: $t_{\text{comb}} = t_{\text{XOR}}$
  - Q2 to D3: $t_{\text{comb}} = t_{\text{AND}} + t_{\text{XOR}}$
  - Q3 to D3: $t_{\text{comb}} = t_{\text{XOR}}$

$$t_{\text{comb}}(Q_i, D_j) = (j - i) \times t_{\text{AND}} + t_{\text{XOR}},\ 0 \leq i \leq j \leq 3$$



Timing Analysis of a Counter

f_{max}

- Step 2b: Find the shortest clock period that satisfies the path's setup-time constraint

$$t_{cQ,\max} + t_{\text{comb, max}} + t_{\text{setup}} \leq T_{\text{CLK}} = 1/f_{\text{CLK}}$$

  - Q0 to D0: $t_{cQ,\max} + t_{\text{XOR}} + t_{\text{setup}} = 1 + 1.3 + 0.6 = 2.9 \text{ ns}$
  - Q0 to D1: $t_{cQ,\max} + t_{\text{AND}} + t_{\text{XOR}} + t_{\text{setup}} = 1 + 1.2 + 1.3 + 0.6 = 4.1 \text{ ns}$
  - Q0 to D2: $t_{cQ,\max} + 2t_{\text{AND}} + t_{\text{XOR}} + t_{\text{setup}} = 5.3 \text{ ns}$
  - Q0 to D3: $t_{cQ,\max} + 3t_{\text{AND}} + t_{\text{XOR}} + t_{\text{setup}} = 6.5 \text{ ns}$
  - Q1 to D1: $t_{cQ,\max} + t_{\text{XOR}} + t_{\text{setup}} = 2.9 \text{ ns}$
  - Q1 to D2: $t_{cQ,\max} + t_{\text{AND}} + t_{\text{XOR}} + t_{\text{setup}} = 4.1 \text{ ns}$
  - Q1 to D3: $t_{cQ,\max} + 2t_{\text{AND}} + t_{\text{XOR}} + t_{\text{setup}} = 5.3 \text{ ns}$
  - Q2 to D2: $t_{cQ,\max} + t_{\text{XOR}} + t_{\text{setup}} = 2.9 \text{ ns}$
  - Q2 to D3: $t_{cQ,\max} + t_{\text{AND}} + t_{\text{XOR}} + t_{\text{setup}} = 4.1 \text{ ns}$
  - Q3 to D3: $t_{cQ,\max} + t_{\text{XOR}} + t_{\text{setup}} = 2.9 \text{ ns}$

Timing Analysis of a Counter

f_{max}

- Step 3: Find the shortest clock period T_{CLK} that satisfies the setup-time constraints of all those paths:

$$T_{\text{CLK}} = \max(2.9, 4.1, 5.3, 6.5) = 6.5\ \text{ns}$$

- Compute the highest operating frequency:

Note: max frequency is rounded down

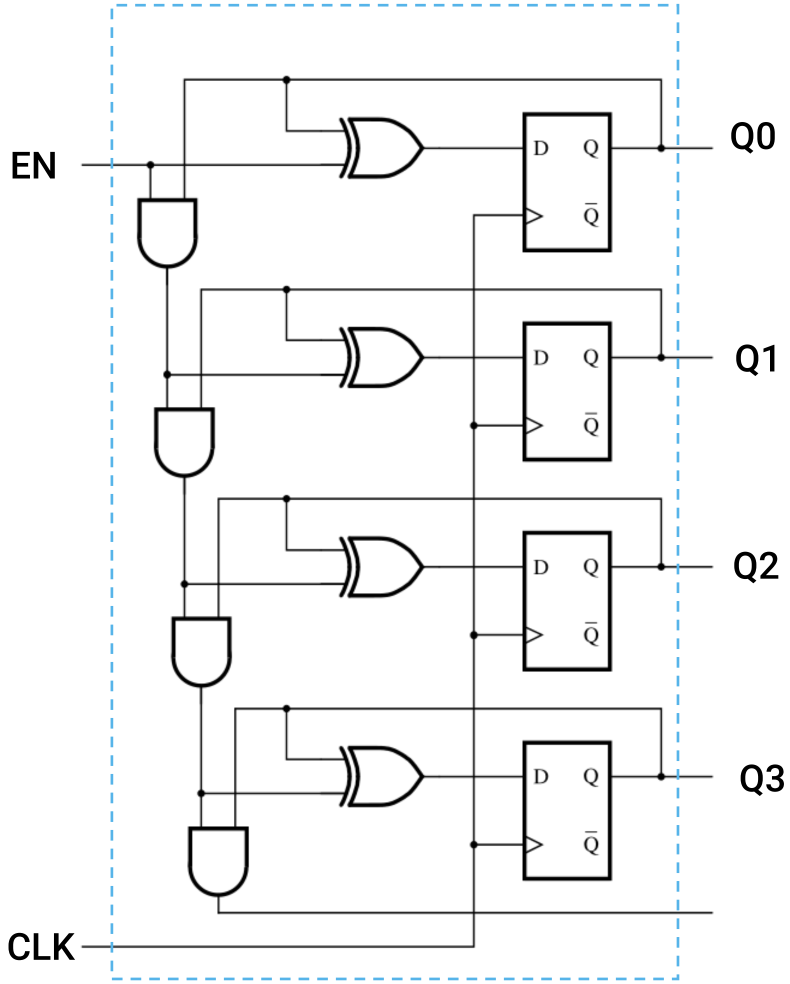
$$f_{\max} = 1/T_{\text{CLK}} = 153\ \text{MHz}$$

Timing Analysis of a Counter

Hold-Time Violations

- Step 1: Identify all Q-to-D paths
- Step 2a: For each of the paths, find shortest combinational delay

No need to repeat these steps in our example, because there is only one path between every Q and D; its delay is unique (therefore, the min equals the max). In another case, however, one should repeat these steps, as there could be multiple paths between every Q and D.



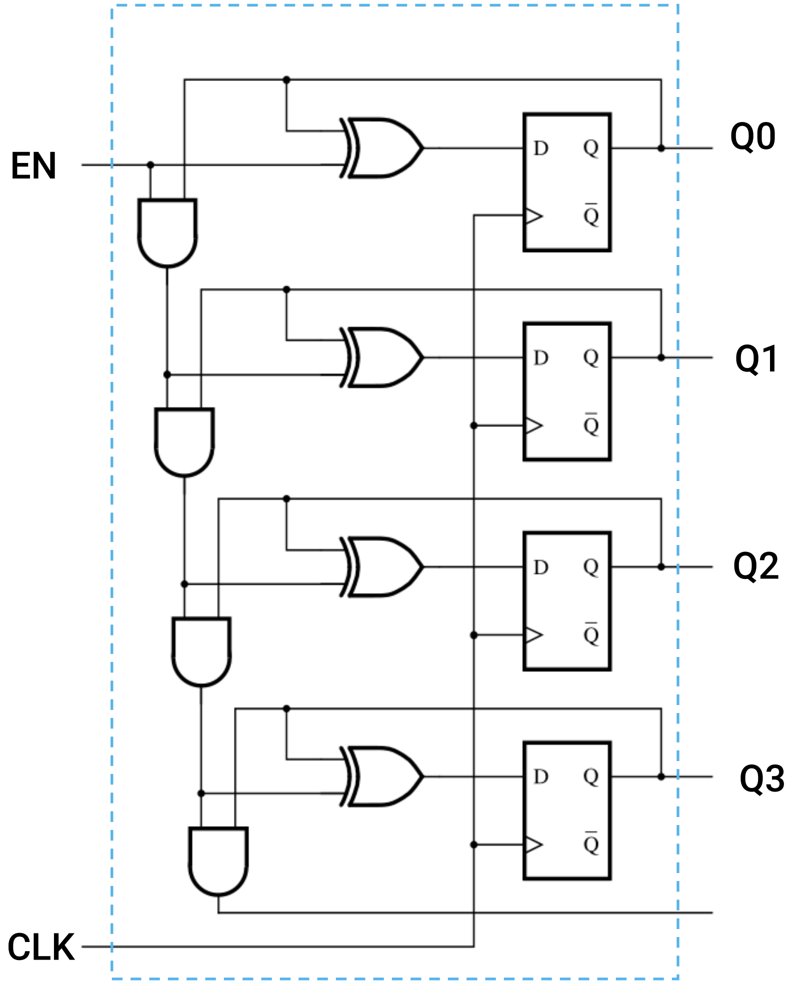
Timing Analysis of a Counter

Hold-Time Violations

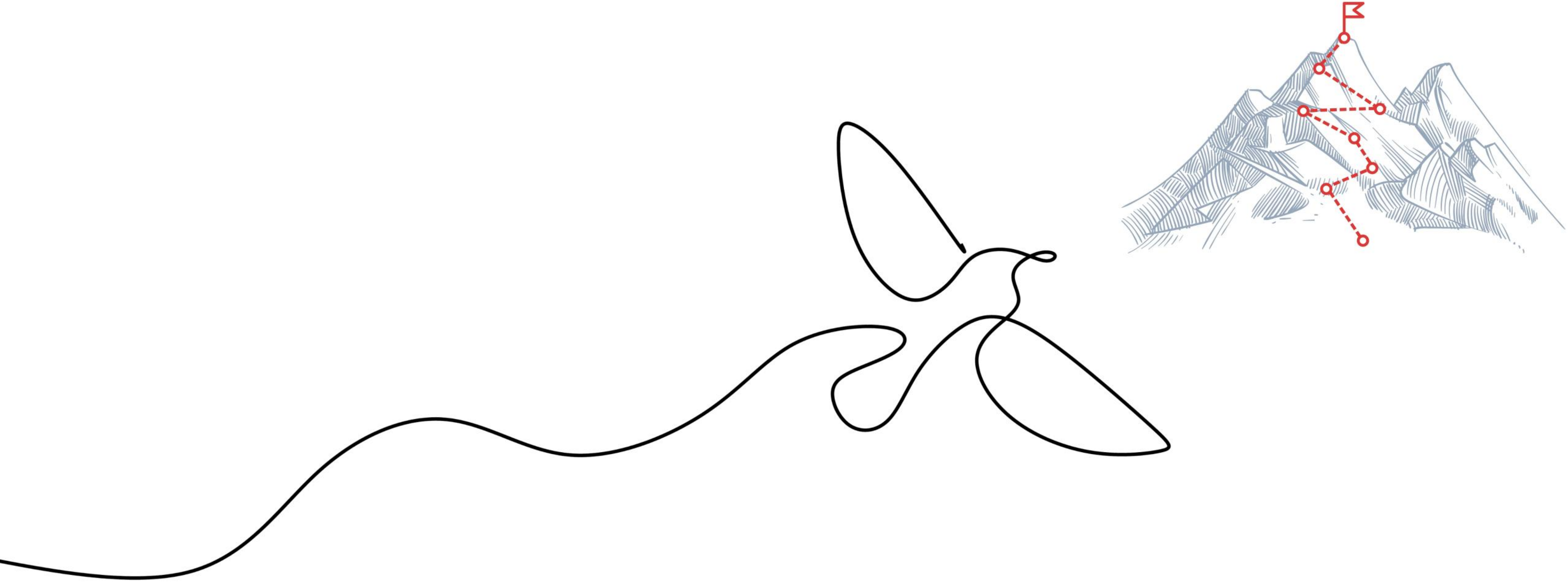
- Step 3: Verify if hold-time constraint is satisfied

$$t_{cQ,\min} + t_{\text{comb, min}} \geq t_{\text{hold}}$$

- Q0 to D0: $t_{cQ,\min} + t_{\text{XOR}} = 2.1 \geq t_{\text{hold}} = 0.4\ \text{ns}$
- Q0 to D1: $t_{cQ,\min} + t_{\text{AND}} + t_{\text{XOR}} = 3.3 \geq 0.4\ \text{ns}$
- Q0 to D2: $t_{cQ,\min} + 2t_{\text{AND}} + t_{\text{XOR}} = 4.5 \geq 0.4\ \text{ns}$
- Q0 to D3: $t_{cQ,\min} + 3t_{\text{AND}} + t_{\text{XOR}} = 5.7 \geq 0.4\ \text{ns}$
- Q1 to D1: Same as Q0 to D0
- Q1 to D2: Same as Q0 to D1
- Q1 to D3: Same as Q0 to D2
- Q2 to D2: Same as Q0 to D0
- Q2 to D3: Same as Q0 to D1
- Q3 to D3: Same as Q0 to D0

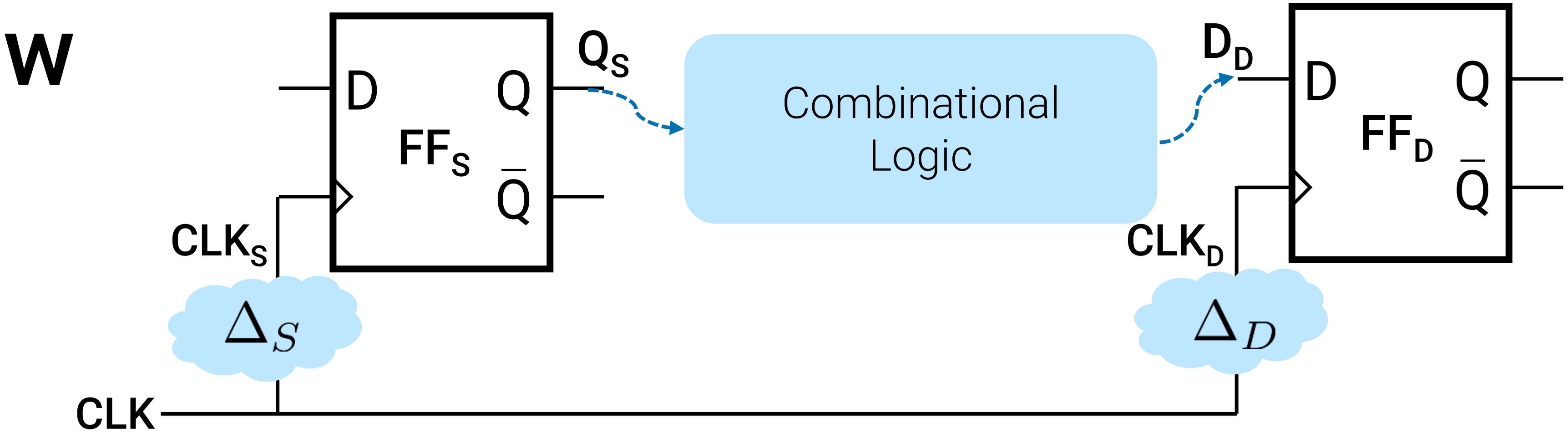


Conclusion: All relevant paths satisfy hold-time constraints



Clock Skew

Clock Skew



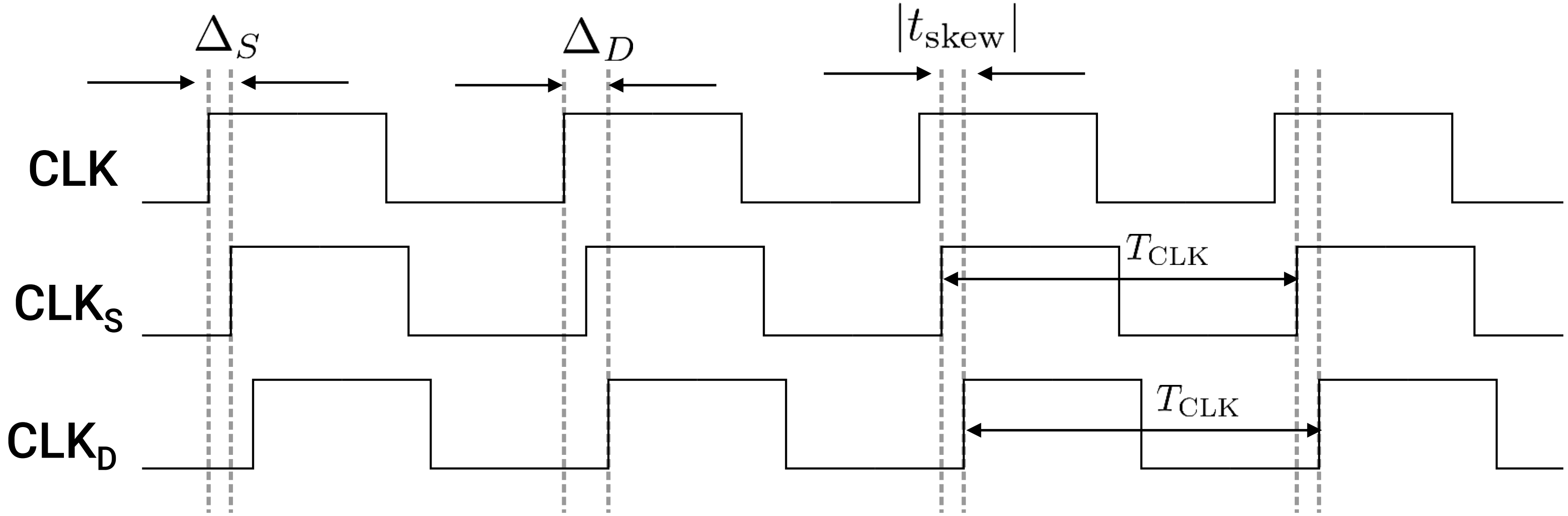
- In real circuits, the clock signal may not arrive at all FFs at the same time because of the variations in the delay of the wires that carry it
- **Variation in the arrival time** of the clock signal between different flip-flops is called **clock skew:**

$$t_{\text{skew}} = \Delta_D - \Delta_S$$

- Δ_i is the arrival time of the clock edge to the FF$_i$
- Clock skew should also be taken into account in the timing analysis

Clock Delays

- Clock arriving to the flip-flops is delayed with respect to the clock source
- For example, assuming $\Delta_D > \Delta_S$:



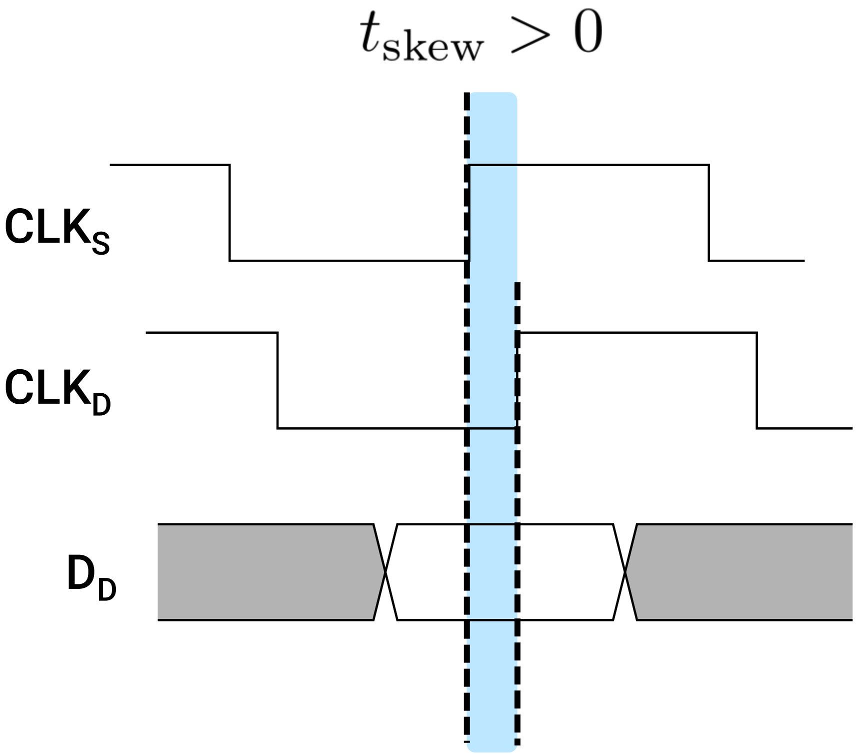
- Clock delays impact the timing of D; they should not be ignored

Clock Skew

Positive

- **Positive** clock skew between CLK$_D$ and CLK$_S$ means that the rising edge of CLK$_D$ is **delayed (late)** with respect to the rising edge of CLK$_S$

$$t_{\text{skew}} = \Delta_D - \Delta_S > 0$$

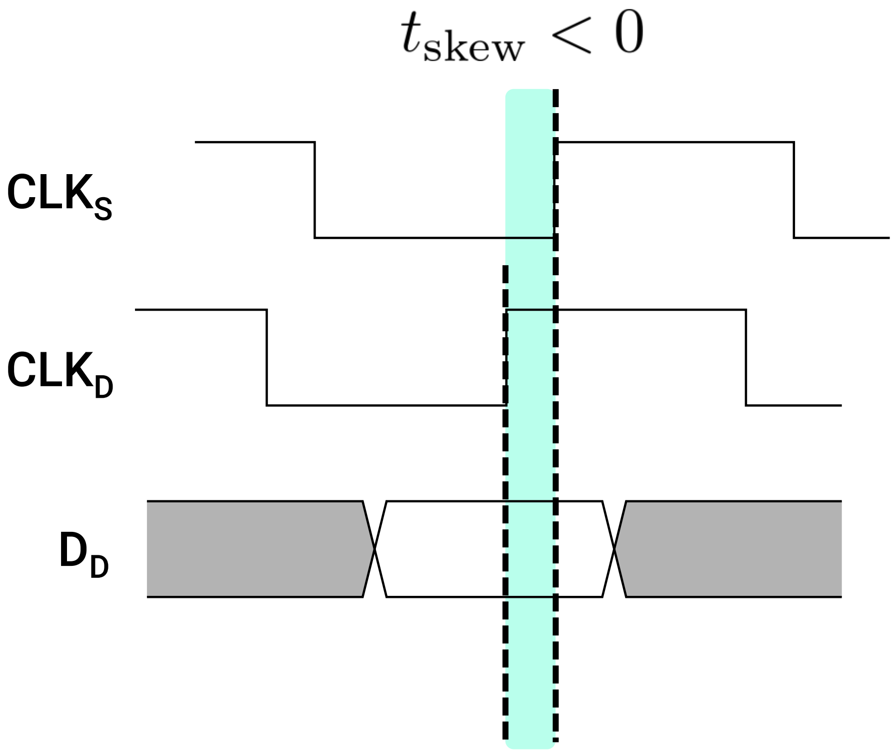


Clock Skew

Negative

- **Negative** clock skew between CLK$_D$ and CLK$_S$ means that the rising edge of CLK$_D$ is **advanced (early)** with respect to the rising edge of CLK$_S$

$$t_{\text{skew}} = \Delta_D - \Delta_S < 0$$



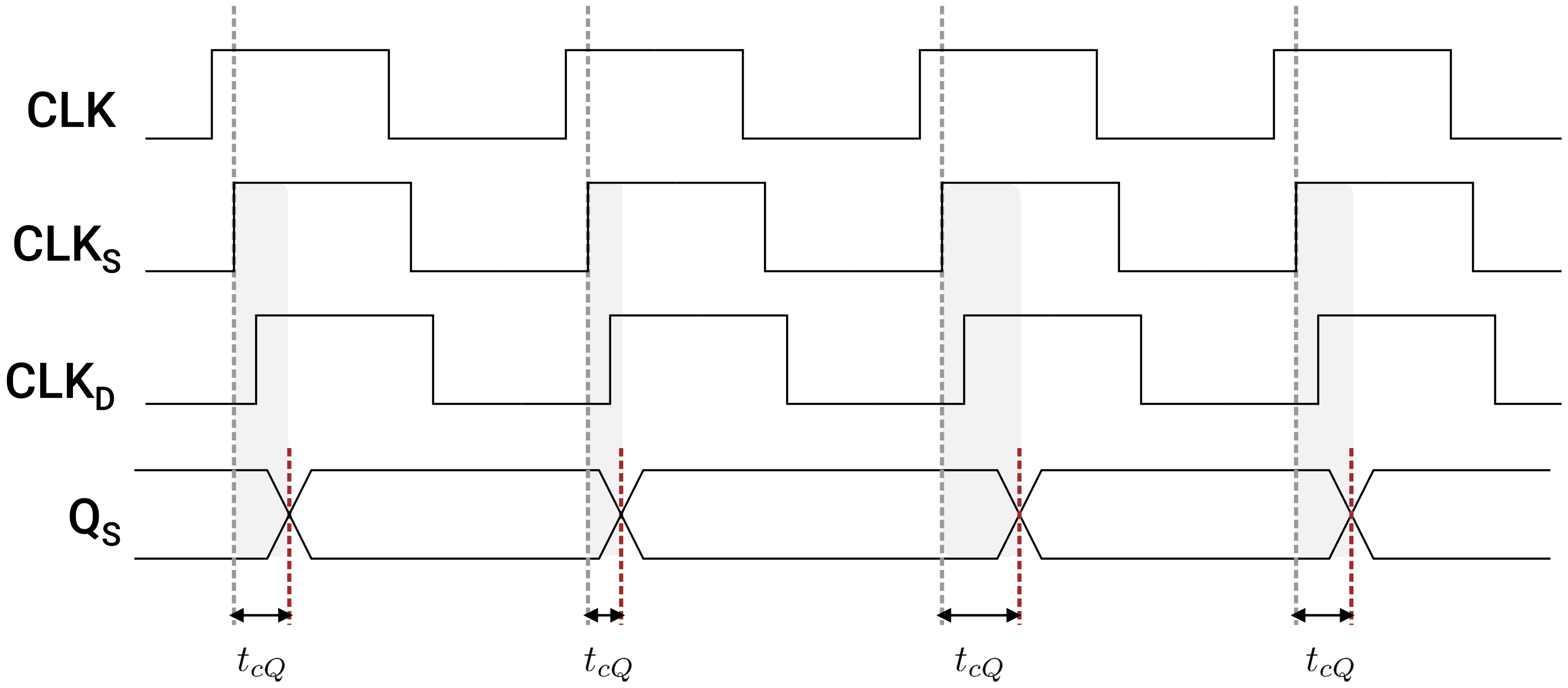
Life of D

In the Presence of Clock Skew

Life of D

In the Presence of Clock Skew

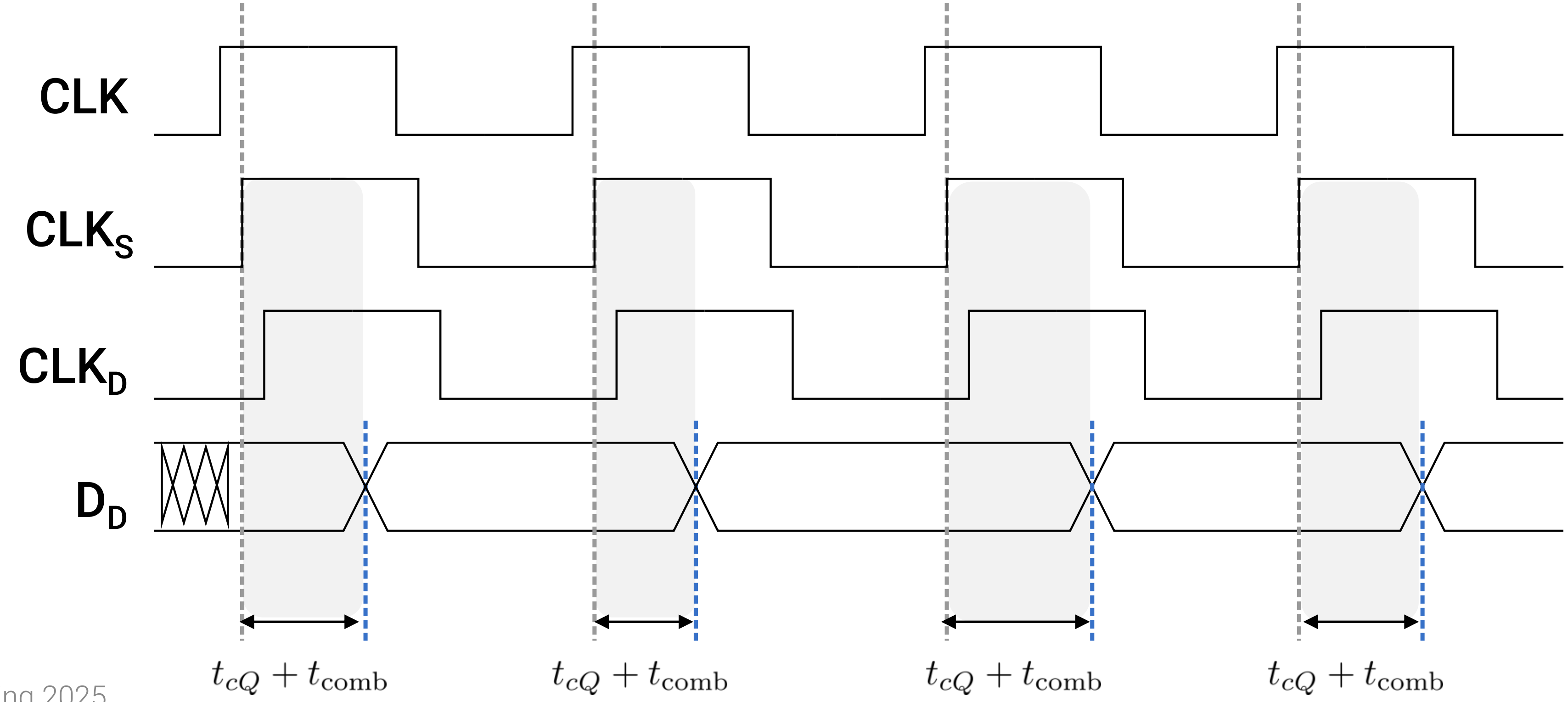
- Born as Q of the source FF: appears after t_{cQ} with respect to CLK$_S$



Life of D

In the Presence of Clock Skew

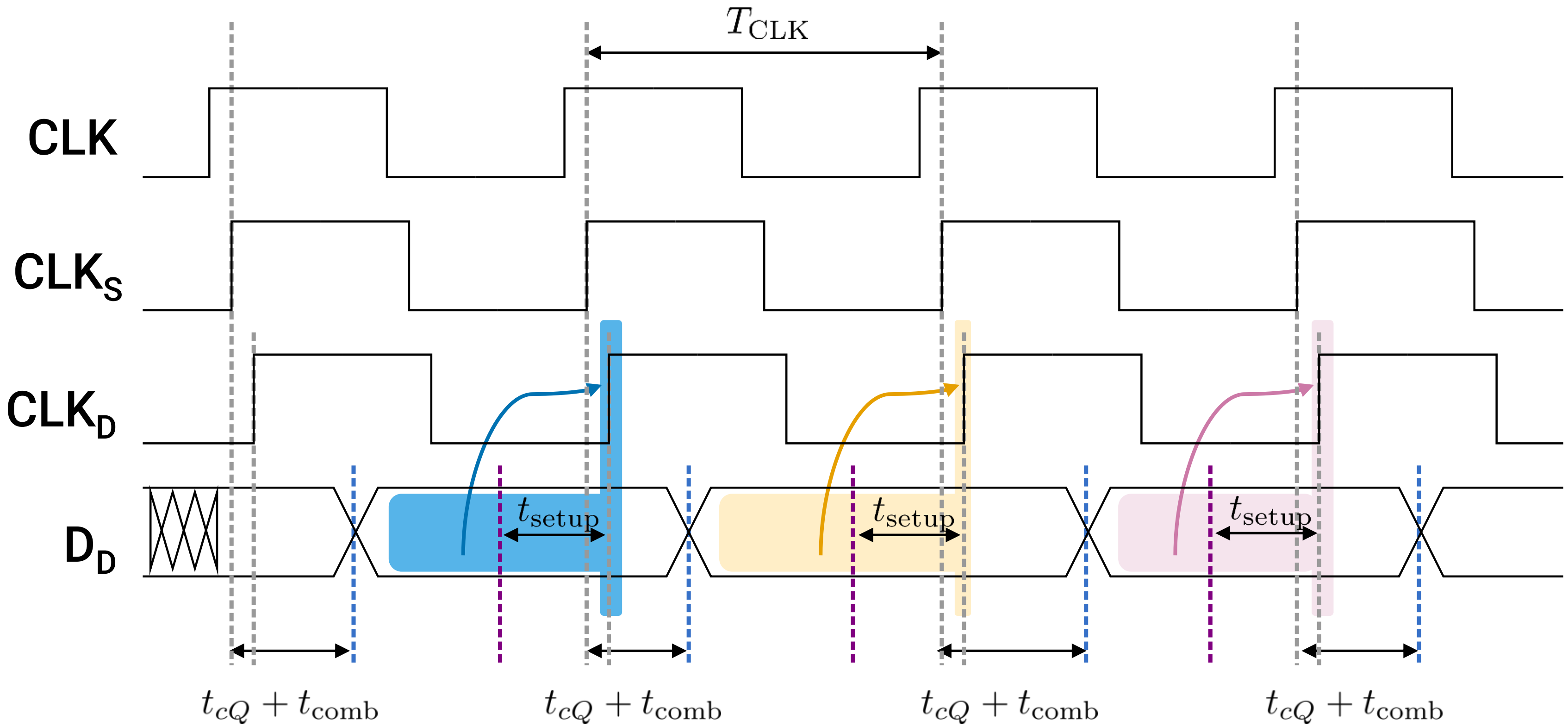
- Journey through the combinational logic: starts as Q_S, arrives as D_D
- Duration of the journey: t_{comb}


CLK
CLK_S
CLK_D
D_D
$t_{cQ} + t_{\text{comb}}$
$t_{cQ} + t_{\text{comb}}$
$t_{cQ} + t_{\text{comb}}$
$t_{cQ} + t_{\text{comb}}$

Life of D

In the Presence of Clock Skew

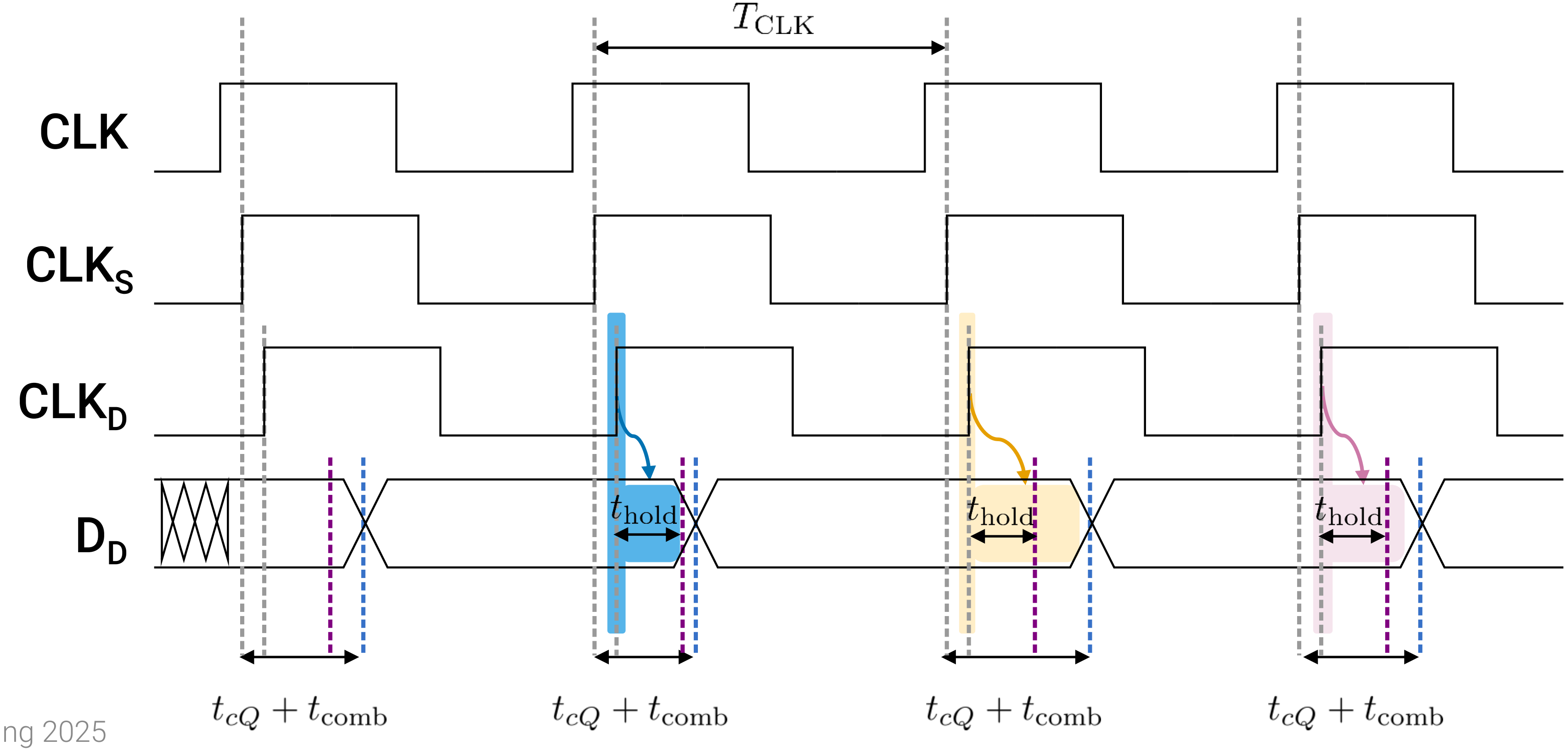
- Waits to be captured at the next rising edge of the clock CLK$_D$ (the clock at the destination FF). The wait time must be at least t_{setup}


T_{CLK}
CLK
CLK$_S$
CLK$_D$
D$_D$
t_{setup}
t_{setup}
t_{setup}
$t_{cQ} + t_{\text{comb}}$
$t_{cQ} + t_{\text{comb}}$
$t_{cQ} + t_{\text{comb}}$
$t_{cQ} + t_{\text{comb}}$

Life of D

In the Presence of Clock Skew

- Gets captured by the next rising clock edge and then waits to be replaced; the "wait" must be at least t_{hold}

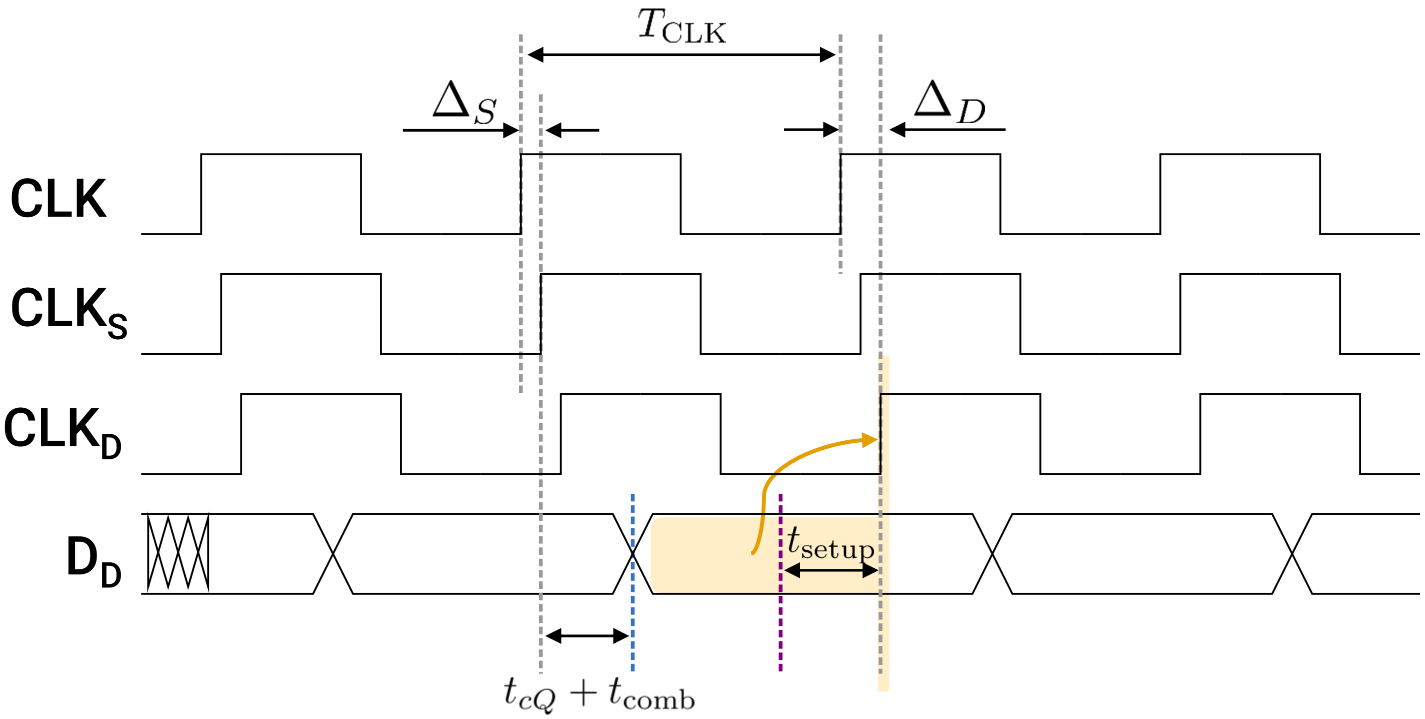


Meeting Timing Constraints

In the Presence of Clock Skew

Meeting Setup-Time Constraints

In the Presence of Clock Skew



- The following expression must hold for all values of t_{cQ} and t_{comb}:

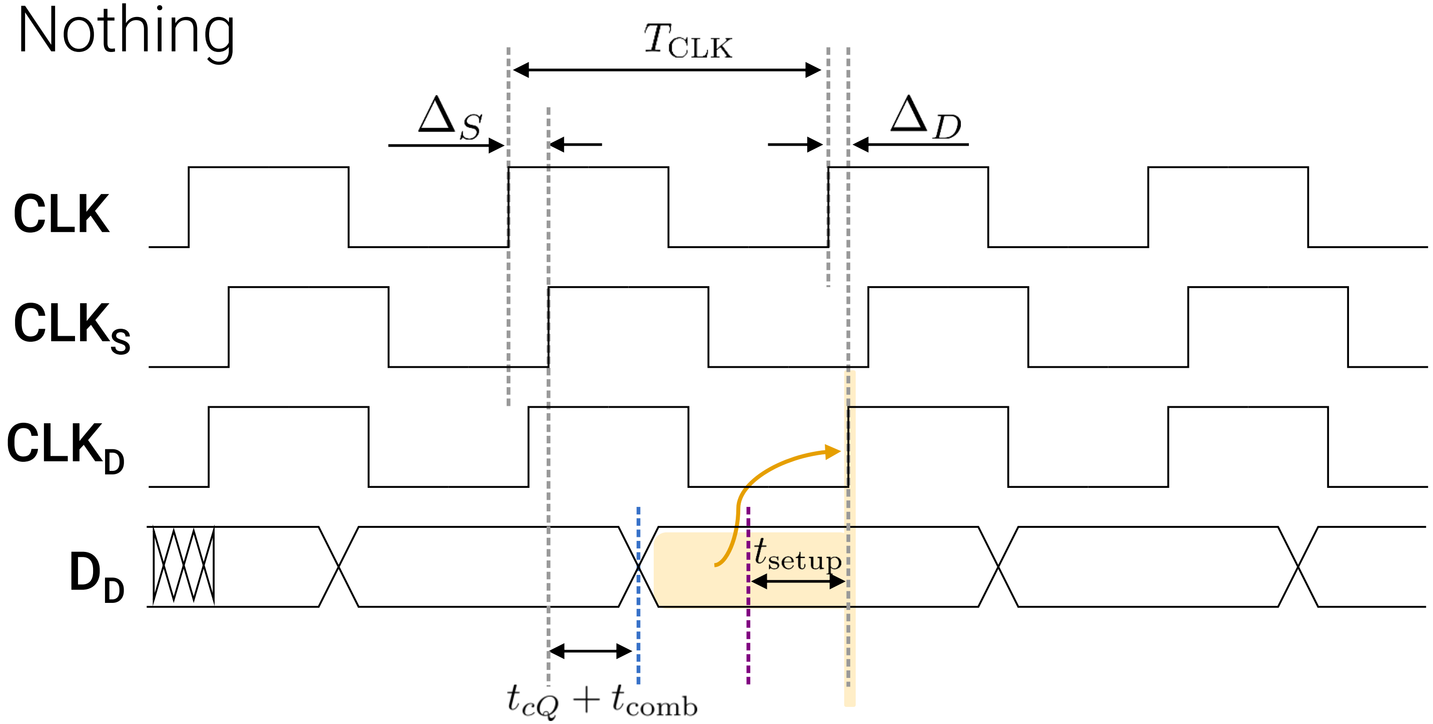
$$T_{\text{CLK}} + \Delta_D - (\Delta_S + t_{cQ} + t_{\text{comb}}) \geq t_{\text{setup}}$$

- The worst-case constraint can be rewritten as

$$t_{cQ,\text{max}} + t_{\text{comb, max}} + t_{\text{setup}} - (\Delta_D - \Delta_S) \leq T_{\text{CLK}} = 1/f_{\text{CLK}}$$

What Changes if $\Delta_D < \Delta_S$

- **Q:** We derived the expression for testing setup-time constraints assuming that $\Delta_S < \Delta_D$. What changes if the relationship is different ($\Delta_D < \Delta_S$)?
- **A:** Nothing



$$T_{\mathrm{CLK}} + \Delta_D - (\Delta_S + t_{cQ} + t_{\mathrm{comb}}) \geq t_{\mathrm{setup}}$$

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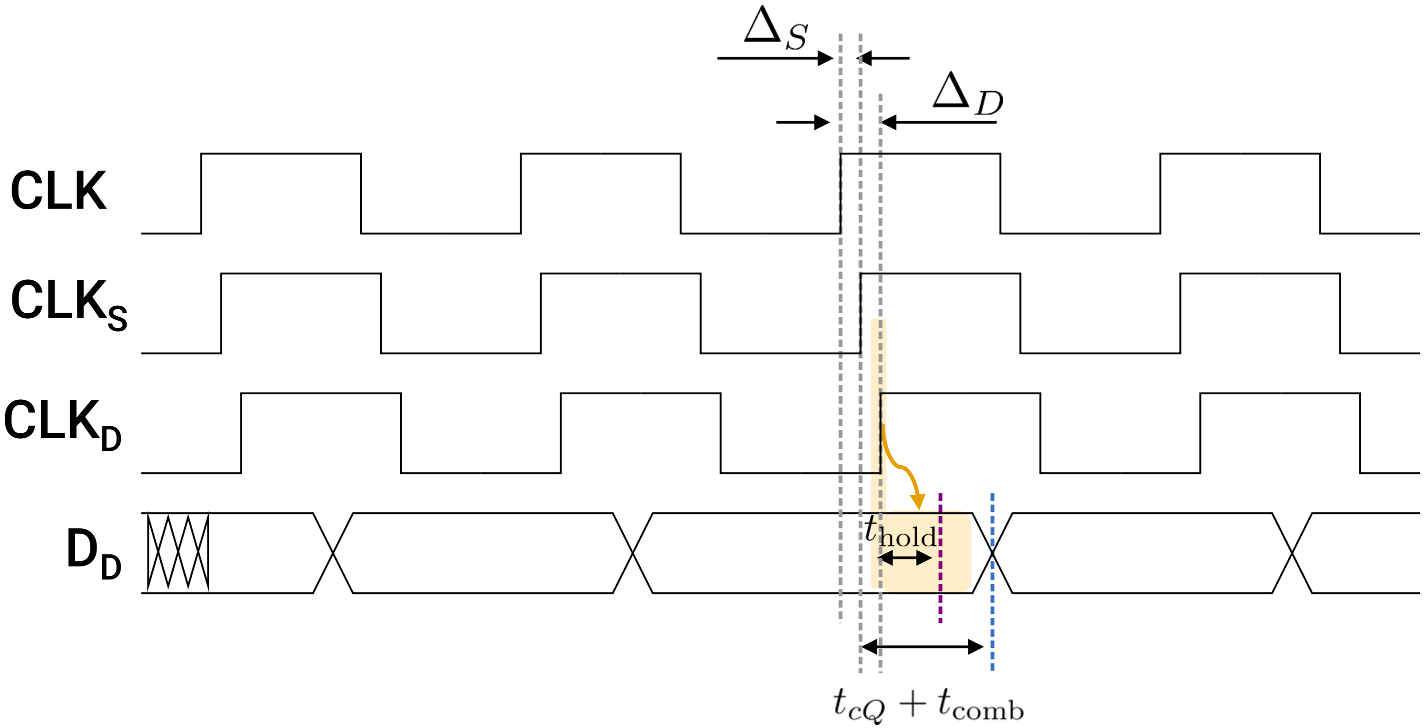
Meeting Hold-Time Constraints

In the Presence of Clock Skew



- The following expression must hold for all possible values of t_{cQ} and t_{comb} :

$$t_{cQ} + t_{\text{comb}} + \Delta_S - \Delta_D \geq t_{\text{hold}}$$

- The worst-case constraint can be rewritten as

$$t_{cQ,\min} + t_{\text{comb},\min} - (\Delta_D - \Delta_S) \geq t_{\text{hold}}$$

Implications of Clock Skew

- On the max operating frequency
- On meeting the hold-time constraints

Implications of Clock Skew

On the Max Operating Frequency

- *Recall:*

$$t_{cQ,\max} + t_{\text{comb, max}} + t_{\text{setup}} - (\Delta_D - \Delta_S) \leq T_{\text{CLK}} = 1/f_{\text{CLK}}$$

- Substituting $t_{\text{skew}} = \Delta_D - \Delta_S$:

$$t_{cQ,\max} + t_{\text{comb, max}} + t_{\text{setup}} - t_{\text{skew}} \leq T_{\text{CLK}} = 1/f_{\text{CLK}}$$

$$t_{cQ,\max} + t_{\text{comb, max}} + t_{\text{setup}} - t_{\text{skew}} = \frac{1}{f_{\max,\text{skew}=0}} - t_{\text{skew}} = \frac{1}{f_{\max}}$$

- **Positive** skew **improves** the max frequency:

$$\frac{1}{f_{\text{max, skew}=0}} > \frac{1}{f_{\max}} \quad \Longrightarrow \quad f_{\max} > f_{\text{max, skew}=0}$$

- **Negative** skew **worsens** the max frequency:

$$\frac{1}{f_{\text{max, skew}=0}} < \frac{1}{f_{\max}} \quad \Longrightarrow \quad f_{\max} < f_{\text{max, skew}=0}$$

What Can One Do…

- **Q1:** …if the circuit cannot work correctly at the desired frequency due to unsatisfied setup-time constraints?

$$t_{cQ,\mathrm{max}} + t_{\mathrm{comb,\ max}} + t_{\mathrm{setup}} - t_{\mathrm{skew}} \leq T_{\mathrm{CLK}} = 1/f_{\mathrm{CLK}}$$

- **A1:** Redesign the combinational logic to reduce the combinational path delay; try to increase the clock skew. In practice, we let computer-aided design tools do this for us.

Implications of Clock Skew

On Meeting the Hold-Time Constraints

- *Recall:*

$$t_{cQ,\mathrm{min}} + t_{\mathrm{comb,min}} - (\Delta_D - \Delta_S) \geq t_{\mathrm{hold}}$$

- Substituting $t_{\mathrm{skew}} = \Delta_D - \Delta_S$

$$t_{cQ,\mathrm{min}} + t_{\mathrm{comb,min}} - t_{\mathrm{skew}} \geq t_{\mathrm{hold}}$$

- **Positive** skew makes meeting hold-time constraints more **difficult**
- **Negative** clock skew makes meeting hold-time constraints **easier**

What Can One Do…

- **Q2:** …if the circuit cannot work correctly due to unsatisfied hold-time constraints?

$$t_{cQ,\mathrm{min}} + t_{\mathrm{comb,min}} - t_{\mathrm{skew}} \geq t_{\mathrm{hold}}$$

- **A2:** Insert buffers on the short combinational paths to increase their delay; try to reduce the clock skew. In practice, we let computer-aided design tools do this for us.

Example: Timing Analysis

In the Presence of Clock Skew

Recall: Algorithm for Finding f_{max}

- Algorithm for finding f_{max}
  1. Identify all Q-to-D paths
  2. For every such path
     a. Compute its longest combinational delay
     b. Find the shortest clock period that satisfies the path's setup-time constraint
        Remember to include clock delays in the expressions
  3. Find the shortest clock period T_{CLK} that satisfies the setup-time constraints of **all** those paths
  4. Compute $f_{max} = 1/T_{CLK}$

Timing Analysis with Clock Skew

f_{max}

- FF timing parameters
  (same as in the previous examples)
  - $t_{\text{setup}} = 0.6 \text{ ns}; t_{\text{hold}} = 0.4 \text{ ns}$
  - $0.8 \text{ ns} \leq t_{\text{cQ}} \leq 1 \text{ ns}$

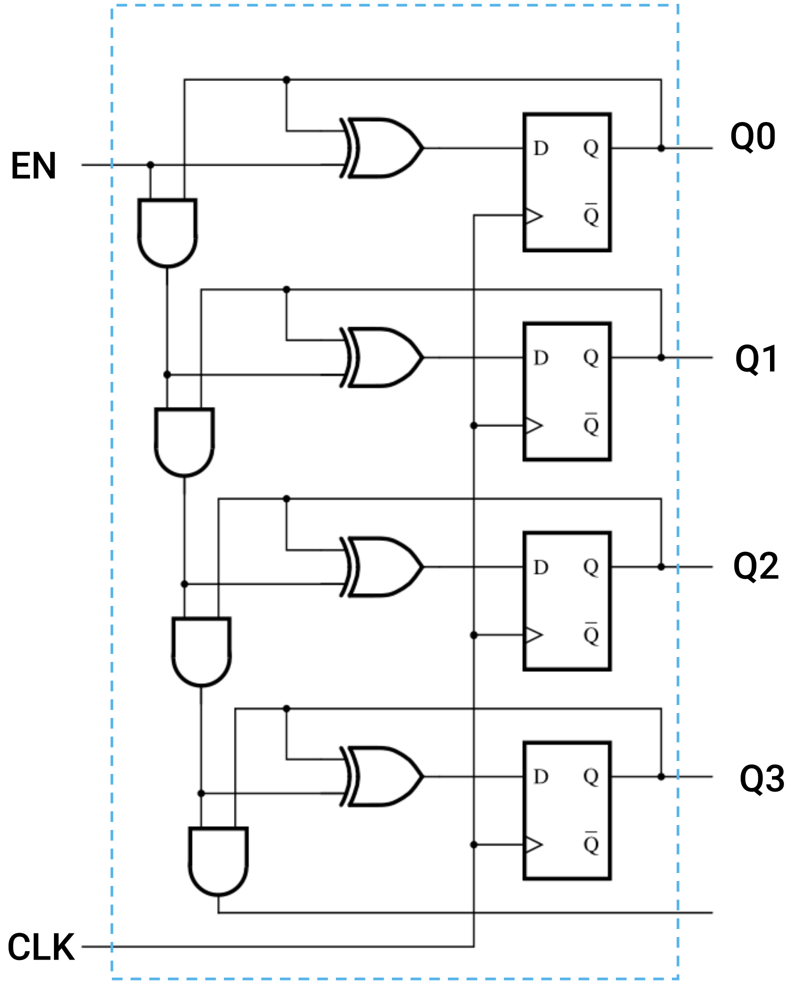
  and gate delays $t_{\text{AND}} = 1.2 \text{ ns}$ and $t_{\text{XOR}} = 1.3 \text{ ns}$

  Assume clock delays:

$$\Delta_0 = 0 \quad \Delta_1 = 0 \quad \Delta_2 = 0 \quad \Delta_3 = 2 \text{ ns}$$

(a) Find the max operating frequency f_{max}

(b) Are there hold-time violations in this circuit?



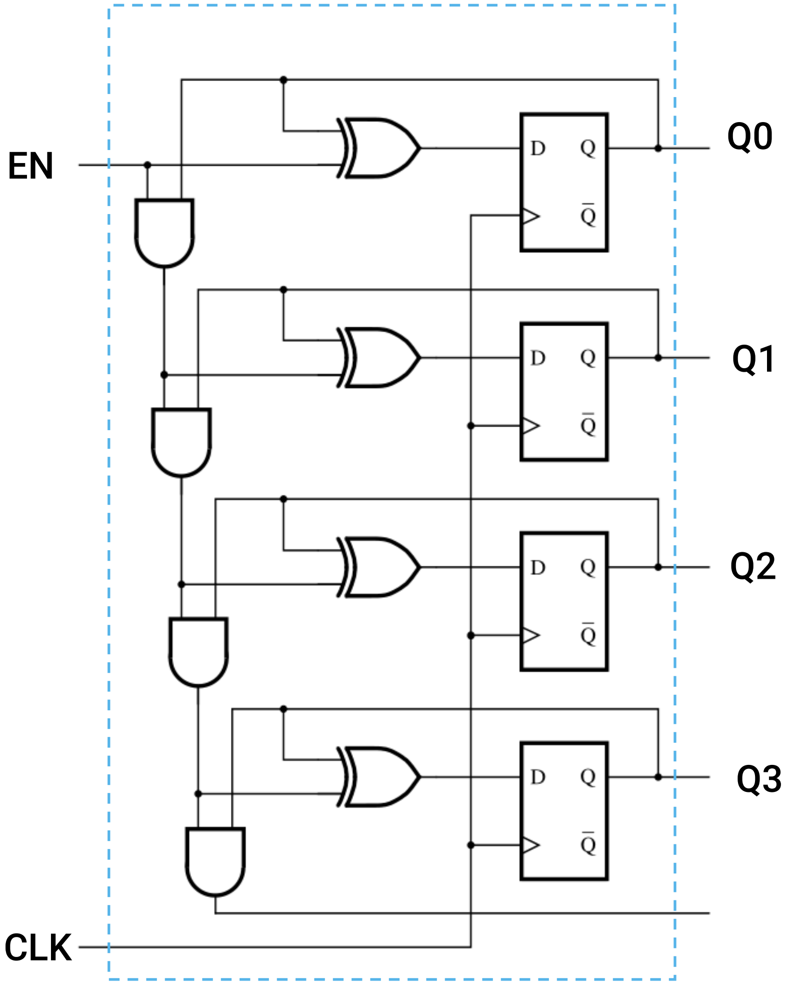
Note: For simplicity, we will assume that EN is available at the rising clock edge

EXAMPLES

Timing Analysis with Clock Skew

f_{max}

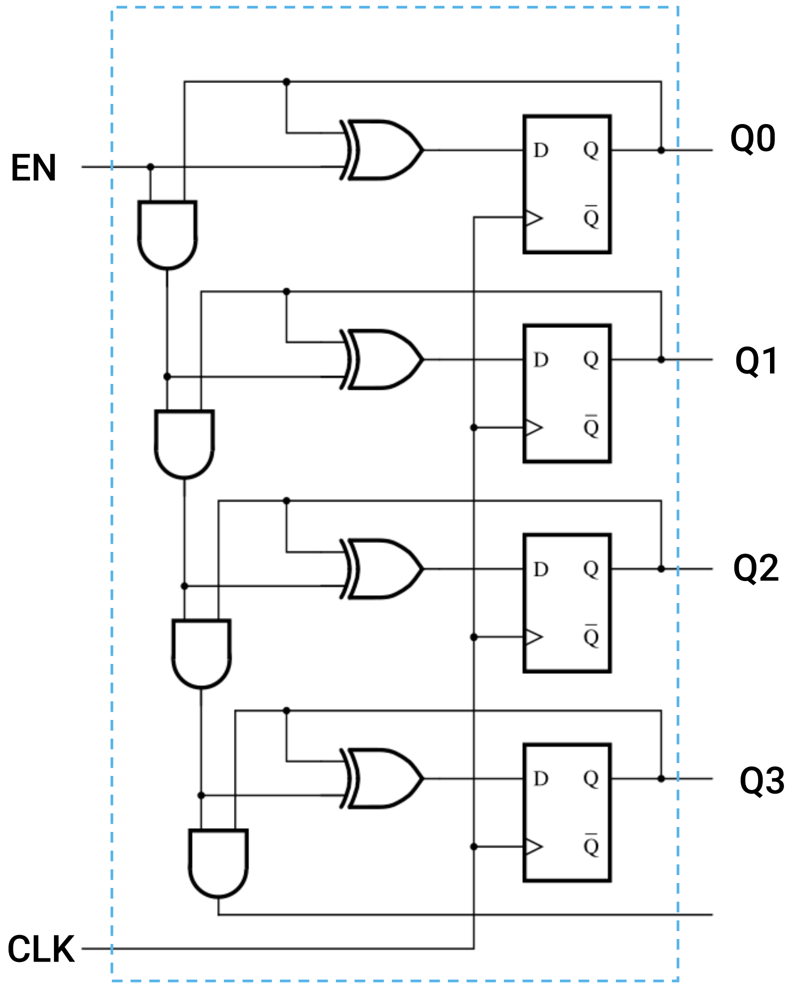
- Step 1: Identify all Q-to-D paths
- We already computed delays of all paths (see earlier example); let us focus on only the paths affected by clock delays
- As clock at FF3 is delayed, the Q-to-D paths starting or ending at FF3 are the only ones affected
    - Q0 to D3
    - Q1 to D3
    - Q2 to D3
    - Q3 to D3



Timing Analysis with Clock Skew

f_{max}

- Step 2a: For all paths, find the longest combinational path delay
  - Q0 to D3: $t_{\text{comb}} = 3 \times t_{\text{AND}} + t_{\text{XOR}} = 3 \times 1.2 + 1.3 = 4.9 \text{ ns}$
  - Q1 to D3: $t_{\text{comb}} = 2 \times t_{\text{AND}} + t_{\text{XOR}} = 2 \times 1.2 + 1.3 = 3.7 \text{ ns}$
  - Q2 to D3: $t_{\text{comb}} = t_{\text{AND}} + t_{\text{XOR}} = 1.2 + 1.3 = 2.5 \text{ ns}$
  - Q3 to D3: $t_{\text{comb}} = t_{\text{XOR}} = 1.3 \text{ ns}$



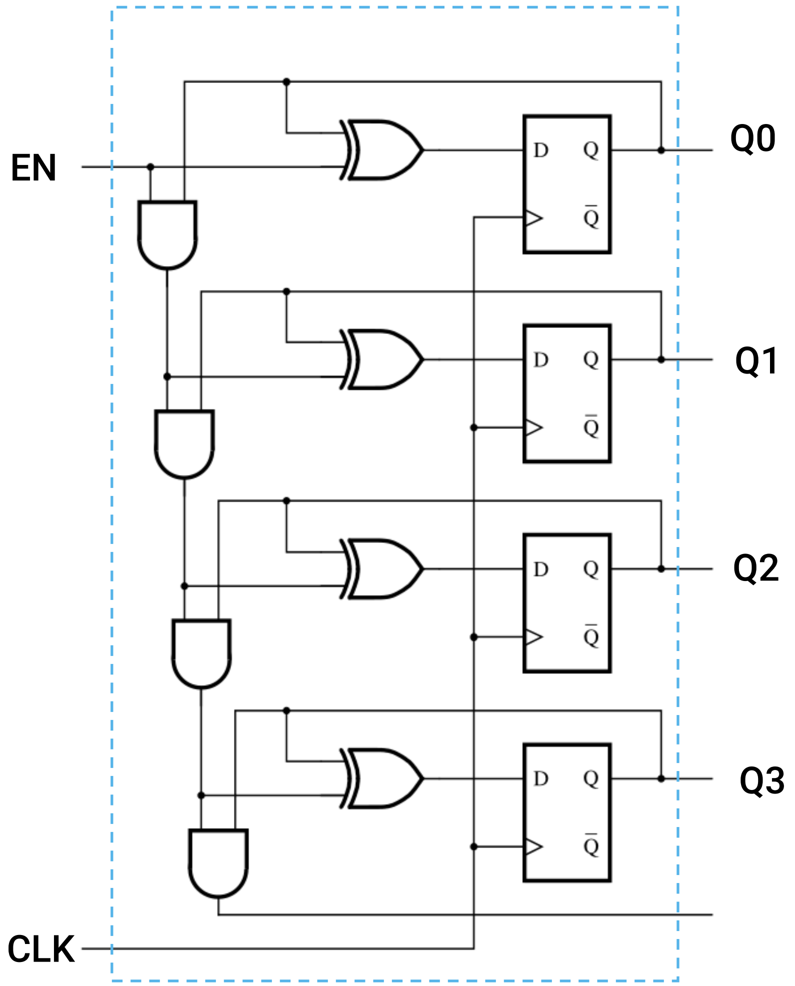
Timing Analysis with Clock Skew

f$_{max}$

- Step 2b: Find the shortest clock period that satisfies the path's setup-time constraint
  Remember to include clock skew in the expressions

$$t_{cQ,\max} + t_{\mathrm{comb},\max} + t_{\mathrm{setup}} - (\Delta_D - \Delta_S) \leq T_{\mathrm{CLK}}$$

- Q0 to D3: $1 + 4.9 + 0.6 - (2 - 0) = 4.5\ \mathrm{ns}$
- Q1 to D3: $1 + 3.7 + 0.6 - (2 - 0) = 3.3\ \mathrm{ns}$
- Q2 to D3: $1 + 2.5 + 0.6 - (2 - 0) = 2.1\ \mathrm{ns}$
- Q3 to D3: $1 + 1.3 + 0.6 - (2 - 2) = 2.9\ \mathrm{ns}$



Timing Analysis with Clock Skew

f_{max}

- Step 3: Find the shortest period that satisfies all paths
  - Clock period that satisfies all paths involving FF3:

$$\max\left(4.5, 3.3, 2.1, 2.9\right) = 4.5 \text{ ns}$$

  - Clock period that satisfies other paths is determined by the path with the longest combinational delay:
    Q0 to D2: $t_{\text{comb}} = 2 \times t_{\text{AND}} + t_{\text{XOR}} = 2 \times 1.2 + 1.3 = 3.7 \text{ ns}$

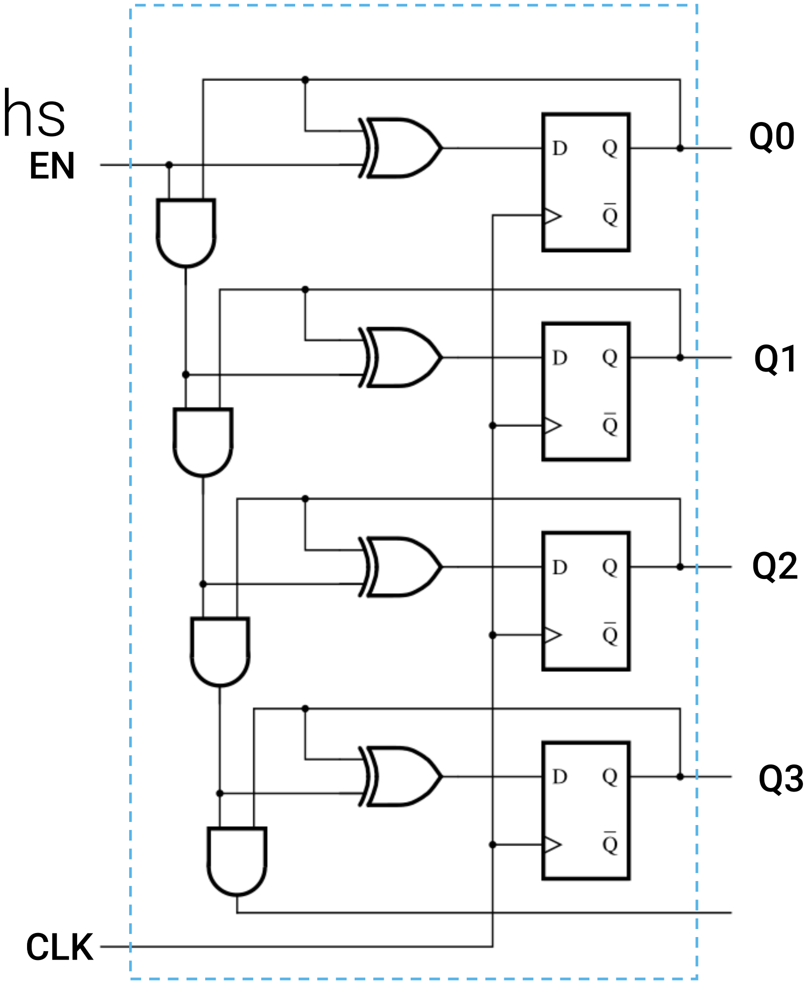
    Q0 to D2: $1 + 3.7 + 0.6 + (0 - 0) = 5.3 \text{ ns}$

  - Finally, the shortest clock period that satisfies all paths

$$T_{\text{CLK}} = \max(4.5, 5.3) = 5.3 \text{ ns}$$

- The max operating frequency is

$$f_{\max} = 1/T_{\text{CLK}} = 188 \text{ MHz}$$



Recall: Algorithm for Checking Hold-Time Violations

- Algorithm for checking if hold-time constraints are satisfied
  1. Identify all Q-to-D paths
  2. For every such path
     a. Compute its shortest combinational delay
     b. Verify if hold-time constraint is satisfied
        Remember to include clock delays in the expressions

Hold-time constraints must be satisfied
for all Q-to-D paths

Timing Analysis with Clock Skew

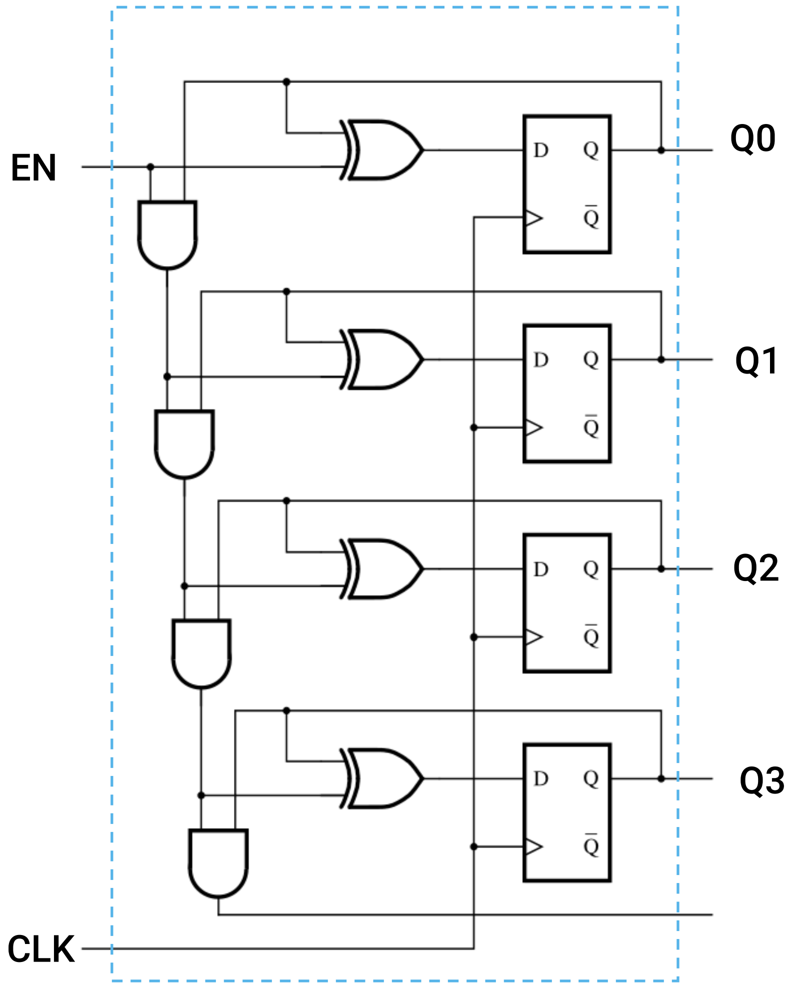
Hold-Time Violations

- Step 1: Identify all Q-to-D paths

  We already verified hold-time constraints for all paths (see earlier example); Therefore, we now focus only on the paths involving FF3, because clock at FF3 is delayed

Step 2a: Find min combinational path delay

- Q0 to D3: $t_{\text{comb}} = 3 \times t_{\text{AND}} + t_{\text{XOR}} = 3 \times 1.2 + 1.3 = 4.9 \text{ ns}$
- Q1 to D3: $t_{\text{comb}} = 2 \times t_{\text{AND}} + t_{\text{XOR}} = 2 \times 1.2 + 1.3 = 3.7 \text{ ns}$
- Q2 to D3: $t_{\text{comb}} = t_{\text{AND}} + t_{\text{XOR}} = 1.2 + 1.3 = 2.5 \text{ ns}$
- Q3 to D3: $t_{\text{comb}} = t_{\text{XOR}} = 1.3 \text{ ns}$



EXAMPLES

Timing Analysis with Clock Skew

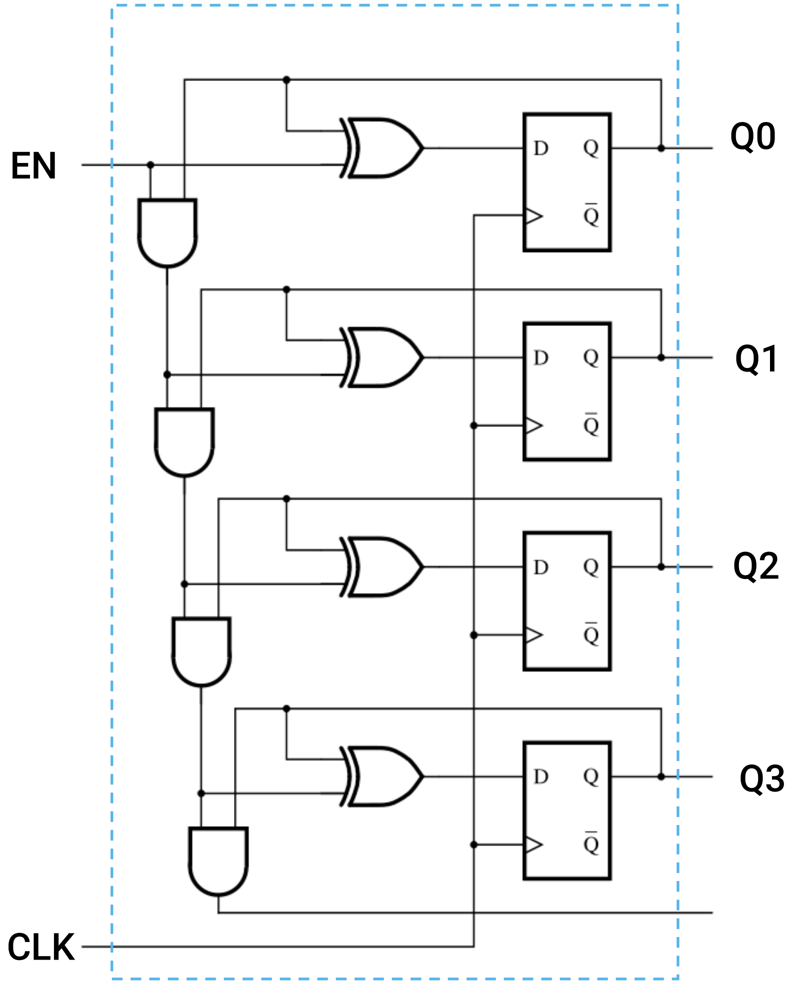
Hold-Time Violations

- Step 2b: Given the clock delay to the source FF, verify if hold-time constraint is satisfied

$$t_{cQ,\text{min}} + t_{\text{comb,min}} - (\Delta_D - \Delta_S) \geq t_{\text{hold}}$$

  - Q0 to D3: $0.8 + 4.7 - (2 - 0) = 3.5 \text{ ns} > 0.4 \text{ ns}$
  - Q1 to D3: $0.8 + 3.7 - (2 - 0) = 2.5 \text{ ns} > 0.4 \text{ ns}$
  - Q2 to D3: $0.8 + 2.5 - (2 - 0) = 1.3 \text{ ns} > 0.4 \text{ ns}$
  - Q3 to D3: $0.8 + 1.3 - (2 - 2) = 2.1 \text{ ns} > 0.4 \text{ ns}$

- Conclusion:
  All relevant paths satisfy hold-time constraints

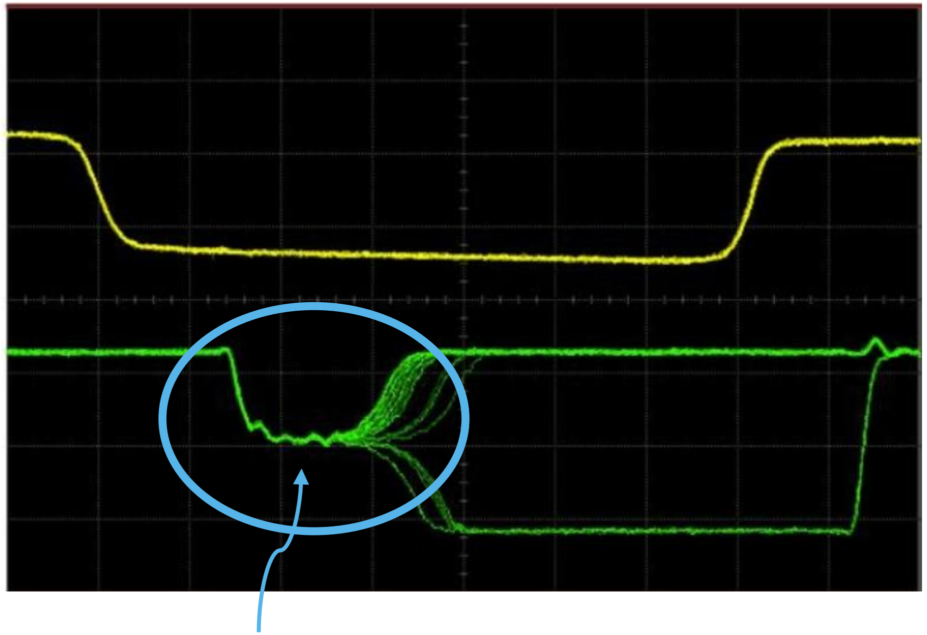


Metastability

Metastability

- If the signal on the data input D of a FF is not stable around the active clock edge (during the setup time or hold time), metastability can occur

- Metastability behavior:
  - First, the output of the FF gets stuck at a voltage level between 0 and 1
  - Later, the output settles to logic 0 or 1, in a nondeterministic (random) manner



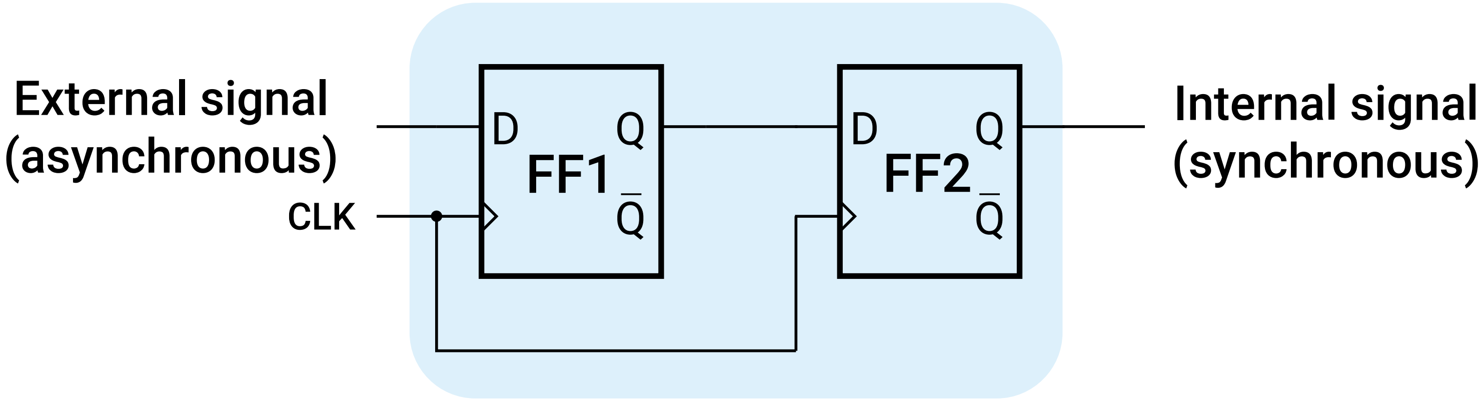
Metastability

Image source: W. J. Dally, Lecture notes
Metastability and Synchronization Failure, 2005

Synchronizer

Shift Register

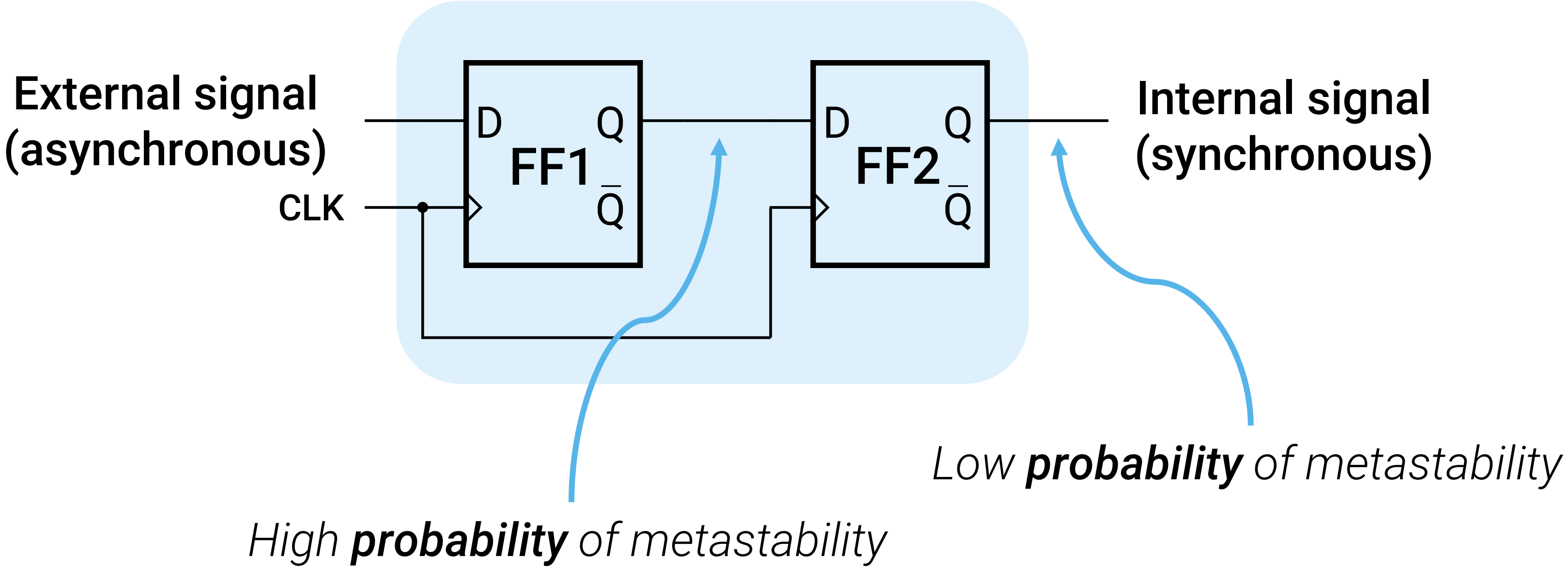
- Metastability concerns input signals that are not synchronous with the clock (e.g., a person pressing a button on the device)
- Easy solution: insert a shift register on the external signal's path

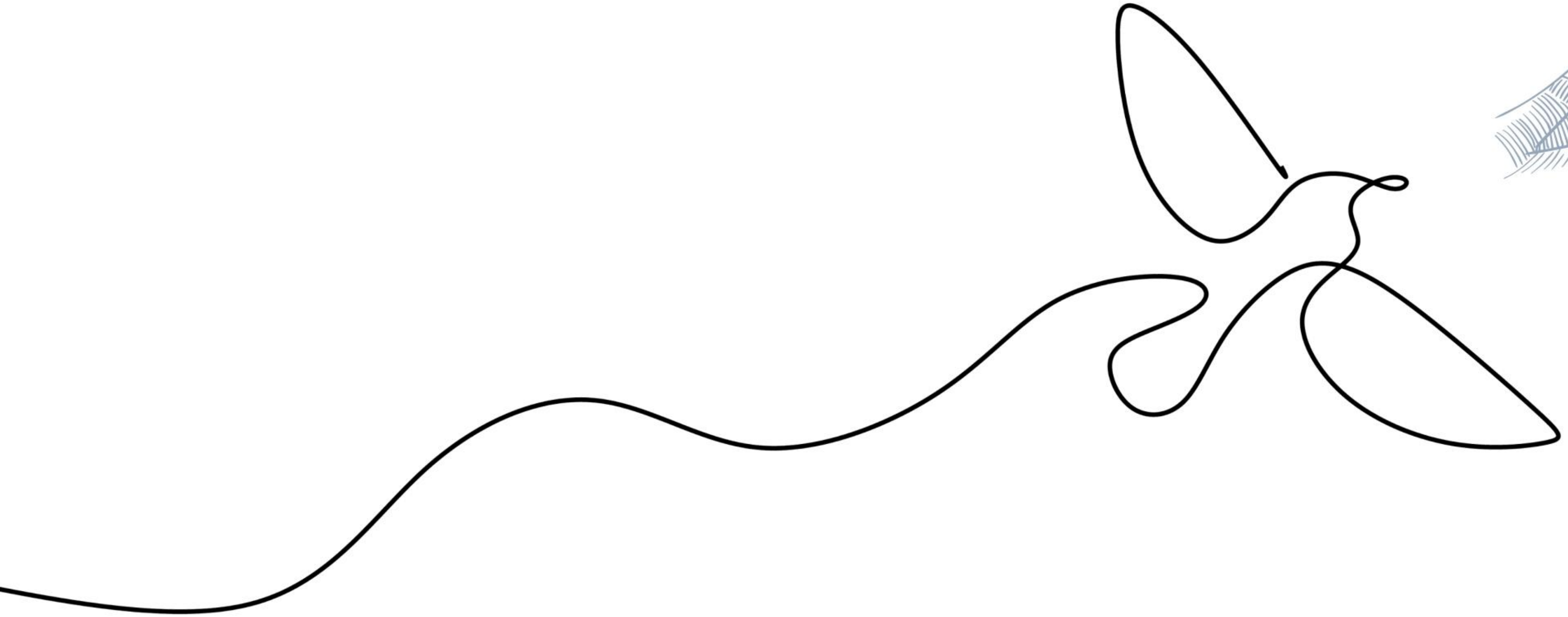


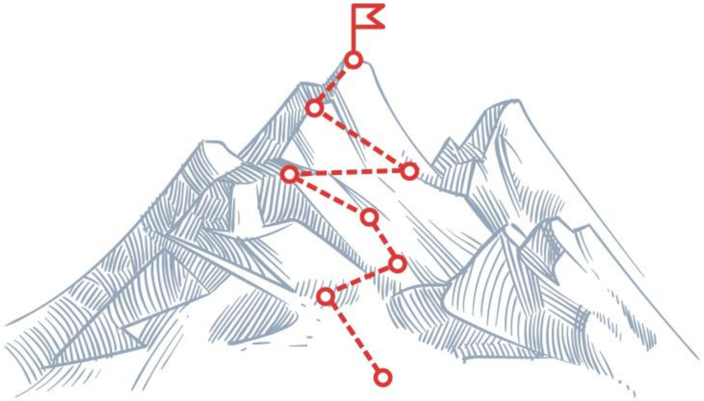
Synchronizer

Shift Register, Contd.

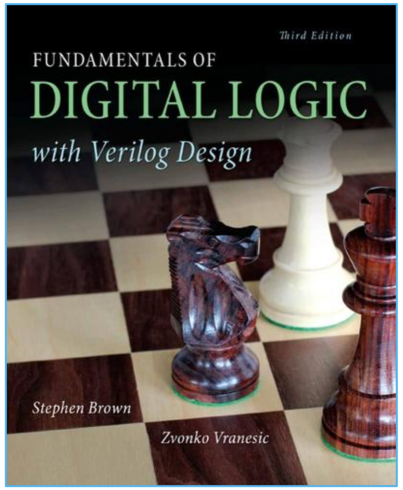
- The output of FF1 is at risk of entering metastability, but if the clock period is long enough, there should be enough time for the output of FF1 to converge to one of the logic values (0 or 1) sufficiently early before the next clock edge. As a consequence, FF2 would operate correctly and prevent the propagation of the metastability to other FFs in the system


External signal (asynchronous)
CLK
D
Q
FF1
Q̄
D
Q
FF2
Q̄
Internal signal (synchronous)
*Low **probability** of metastability*
*High **probability** of metastability*

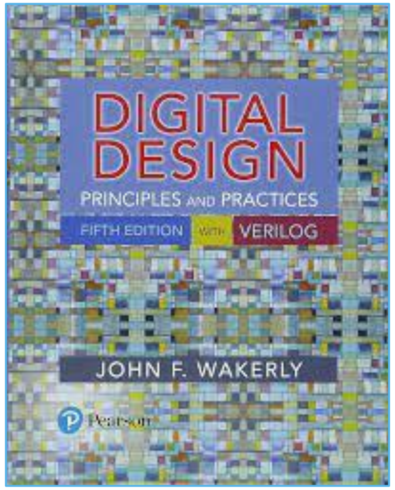




Literature



- Chapter 5: Flip-flops, Registers, and Counters
  - 5.15



- Chapter 13: Sequential-Circuit Design Practices
  - 13.3